## High-breakdown slanted tri-gate gallium nitride power transistors

Researchers claim record figure of merit, reflecting high breakdown and low on-resistance.

un Ma and Elison Matioli of the École Polytechnique Fédérale de Lausanne in Switzerland have used slanted tri-gate structures to enhance the breakdown voltage of gallium nitride (GaN) metal-oxide-semiconductor high-electron-mobility transistors (MOSHEMTs) by 500V [IEEE Electron

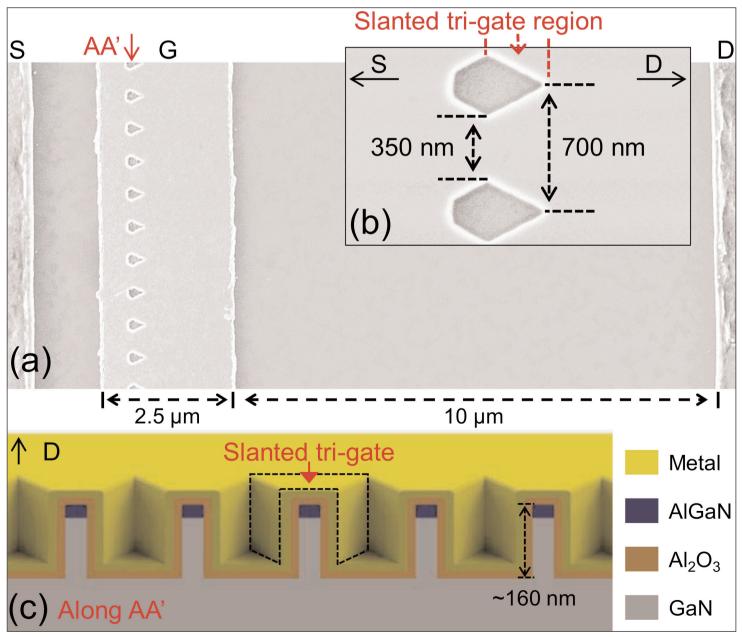


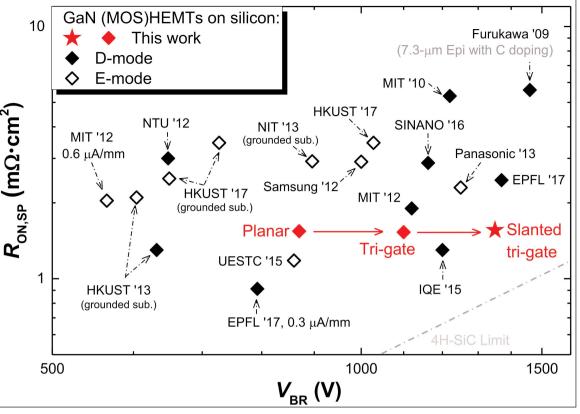
Figure 1. Scanning electron microscope top-view of slanted tri-gate MOSHEMT (a) with and (b) without gate dielectric and metal. (c) Cross-sectional schematic of slanted tri-gate along arrow AA'.

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Device Letters, published online 25 July 2017]. They claim a record 1.2GW/cm<sup>2</sup> highpower figure of merit. The fabricated transistors (Figure 1) consisted of etched nanowires with slanted width within the gate region. The etch depth was 160nm into the aluminium gallium nitride (AlGaN) barrier on gallium nitride channel on silicon structure. The slant gave a 350nm width on the source side and 700nm on the drain side.

The gate stack conaluminium oxide  $(AI_2O_3)$  and metal wrapped around the



sisted of 20nm atomic Figure 2. RoN,SP versus VBR benchmark of slanted tri-gate MOSHEMTs against state-oflayer deposition (ALD) the-art GaN enhancement-mode and depletion-mode (MOS)HEMTs on silicon with breakdown criterion of  $1\mu A/mm$ . R<sub>on.sp</sub> based on  $1.5\mu m$  transfer length for each ohmic contact.  $V_{BR}$  for all reference devices re-calculated based on 1µA/mm criterion.

channel. The source and drain planar sides of the gate were 0.5µm and 1.5µm, respectively. The total gate length was 2.5µm. The source-gate and gate-drain distances were 1.5µm and 10µm, respectively.

Since the researchers were interested in the raw effect of slant gates, they did not use conventional field plates or passivation. In fact, the team sees the tri-gate structure as converting the planar part of the gate towards the drain side into an effective field plate. The slant structure allows the pinch-off potential to vary in such a way that the electric field is kept below critical. The varying potential is mainly achieved by strain relaxation in the AlGaN/GaN nanowires along with the increased electrostatic control offered by the sidewall gates of the tri-gate structure.

Without field plates, or the slant tri-gate structure, the electric field tends to peak at the gate edge on the drain side. However, while field plates require complex processing, tri-gates can be achieved with just one extra etch step.

Even introducing an unslanted tri-gate into the planar transistor improved the breakdown voltage from 877V to 1100V with a  $1\mu$ A/mm leakage criterion. Slanting the tri-gates increased the breakdown further to 1350V, close to the buffer limit, even with a gate-drain distance as low as 10µm.

The off leakage current  $(I_{OFF})$  at lower drain biases

were higher in the slanted tri-gate structure, compared with the planar and unslanted tri-gate MOSHEMTs. The researchers comment: "The larger I<sub>OFF</sub> of the slanted tri-gate device at small voltages is likely due to its much smaller effective gate length, since the three devices have the same buffer leakage current as they were fabricated on the same chip, and exhibited small gate leakage currents  $\leq$  2nA/mm at 750V."

The leakage dependences on bias voltage were similar above 750V up to near the respective breakdowns.

Beyond breakdown characteristics, the slanted trigate structure also exhibited a high on/off current ratio of more than 10<sup>9</sup> and high transconductance up to 72mS/mm at 5V drain bias. The transconductance of the planar device was lower, at 66mS/mm. The onresistance of the devices was similar, at about  $9\Omega$ -mm.

The researchers also compared the slanted tri-gate device with transistors produced by other groups (Figure 2). They point out that their breakdown voltage was comparable with the best reported value of 1460V. At the same time, the specific on-resistance  $(R_{ON,SP})$ was 3.6x lower due to the  $14\mu m$  shorter gate-drain distance in the slanted tri-gate MOSHEMT.

A widely used power transistor figure of merit, V<sub>BR</sub><sup>2</sup>/R<sub>ON,SP</sub>, was 1.2GW/cm<sup>2</sup>, claimed as a record value. ■ https://doi.org/10.1109/LED.2017.2731799 Author: Mike Cooke