

# Balancing charge to boost Ga<sub>2</sub>O<sub>3</sub> breakdown beyond 10kV

Result beats previous Ga<sub>2</sub>O<sub>3</sub> device reports, along with giving thermal stability up to 200°C.

Researchers based mostly in the USA report lateral gallium oxide (Ga<sub>2</sub>O<sub>3</sub>) Schottky barrier diodes (SBDs) with a charge-balancing nickel oxide (NiO) reduced surface field (RESURF) structure that boosted breakdown voltages (BVs) to more than 10kV [Yuan Qin et al, IEEE Electron Device Letters, v44, p1268, 2023]. The BV performance was thermally stable with more than 10kV blocking up to 200°C.

The team from Virginia Polytechnic Institute and State University, University of Southern California, the US Naval Research Laboratory in the USA and Novel Crystal Technology Inc in Japan reports: "Our RESURF Ga<sub>2</sub>O<sub>3</sub> SBDs show the highest BV, and the operational temperature is among the highest in multi-kilovolt Ga<sub>2</sub>O<sub>3</sub> devices."

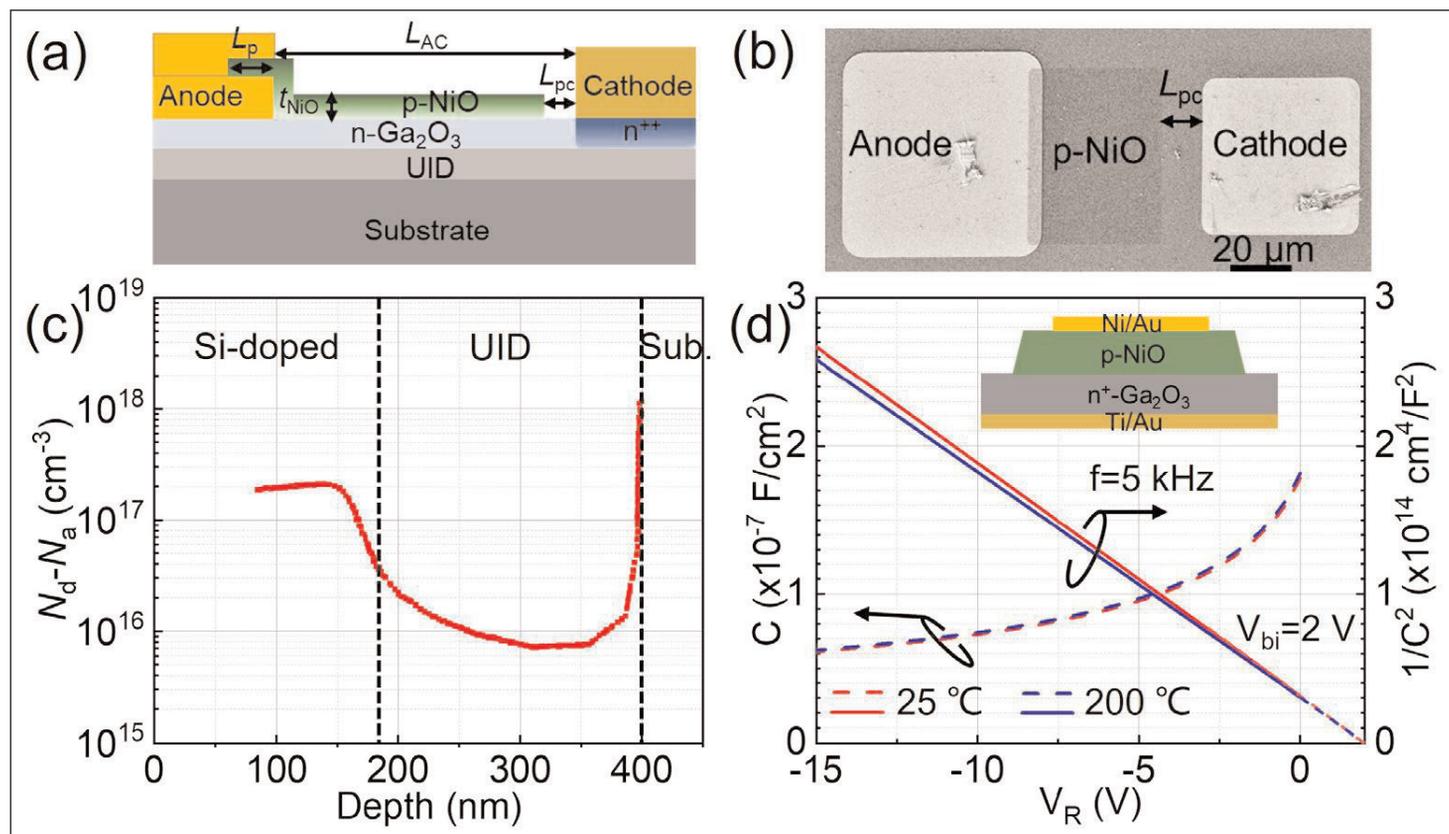
The researchers see potential for their SBD design in medium- and high-voltage, high-temperature applications. The medium-voltage range above 1kV covers deployment

in electric grid, motor drive, and renewable energy processing. The market is presently dominated by silicon bipolar technology, which suffers from slow switching speed.

The SBDs (Figure 1) were fabricated on Ga<sub>2</sub>O<sub>3</sub> substrates with an n-type Ga<sub>2</sub>O<sub>3</sub> epitaxial layer. The anode region doping was boosted using silicon ion implantation, which was activated by 925°C annealing in nitrogen. The cathode was titanium/gold (Ti/Au) annealed at 475°C, and the anode nickel/gold (Ni/Au). Between the cathode and anode formations, the device region was isolated using nitrogen ion implantation.

The aim of the sputtered NiO RESURF structure was to balance depletion charges in the n-Ga<sub>2</sub>O<sub>3</sub> channel at high voltage. Depletion at high forward bias shrinks the effective cross-sectional area for current flow, increasing on-resistance (R<sub>on</sub>).

The p-type hole concentration of NiO has been found



**Figure 1.** (a) Schematic cross-section and (b) top-view scanning electron microscope (SEM) image of fabricated lateral Ga<sub>2</sub>O<sub>3</sub> RESURF SBD. (c)  $N_d - N_a$  depth profile of Ga<sub>2</sub>O<sub>3</sub> epilayers (initial depletion width of Schottky contact  $\sim 85$ nm). (d) Capacitance–voltage (C–V) and  $1/C^2$ –V characteristics of vertical NiO/Ga<sub>2</sub>O<sub>3</sub> diode at 25°C and 200°C.

to be controlled via the oxygen partial pressure during sputtering. The researchers comment: "To reduce the impact of  $t_{\text{NiO}}$  variation on charge balance and enable a larger process latitude, a lower  $N_a$  is preferred." The team used a pure argon atmosphere, to reduce the hole concentration as much as possible, and the sputtering from a NiO

source was carried out at room temperature. The p-NiO was annealed at 275°C in nitrogen gas.

From capacitance–voltage measurements on a p-NiO/n-Ga<sub>2</sub>O<sub>3</sub> vertical p-n heterojunction diode, the researchers estimate that the acceptor concentration ( $N_a$ ) from the NiO sputtering process was  $8 \times 10^{17}/\text{cm}^3$  at 25°C.

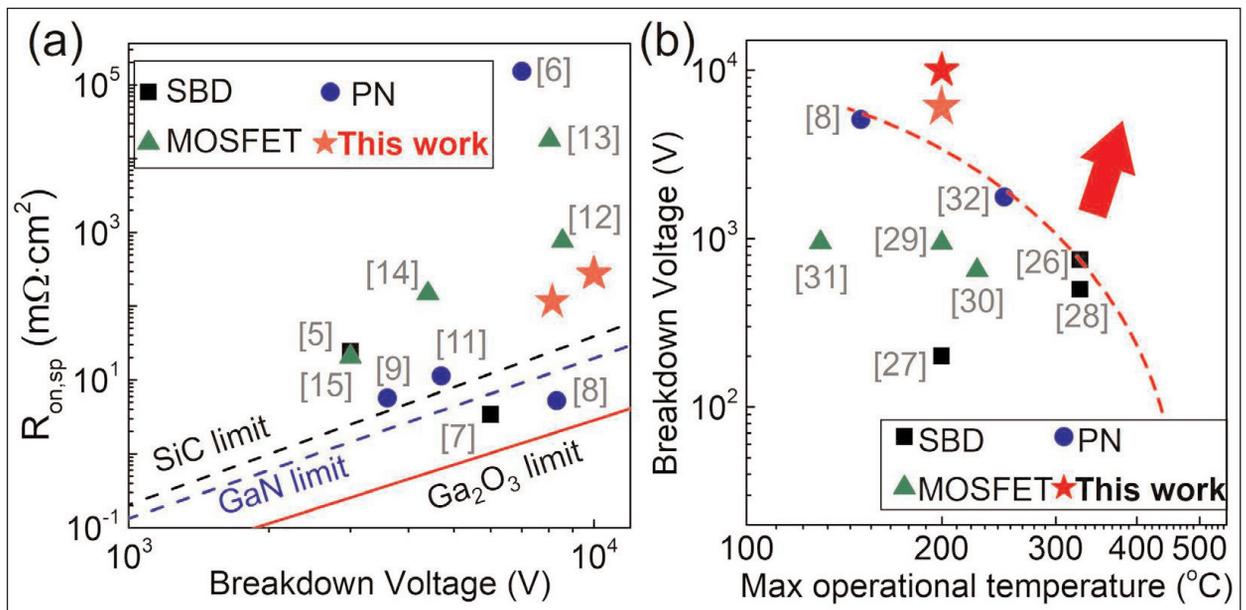
The thickness of the NiO device RESURF layer ( $t_{\text{NiO}}$ ) was designed to keep the charge imbalance margin below 15%. There was also a gap ( $L_{\text{pc}}$ ) between the p-NiO RESURF layer and the cathode to avoid punch-through and leakage conduction. The NiO material was also extended onto the anode surface to a distance of 5  $\mu\text{m}$ . The anode was then covered with a second Ni/Au application.

The device was then annealed at 275°C to stabilize the acceptor concentration and to reduce NiO/Ga<sub>2</sub>O<sub>3</sub> interface states. Passivation with photoresist completed the SBD processing.

A 75nm NiO RESURF layer enabled the team's SBDs with anode–cathode distances ( $L_{\text{AC}}$ ) of 30  $\mu\text{m}$  and 50  $\mu\text{m}$  to exceed 10kV breakdown voltage, the measurement limit of the test equipment. The average electric field ( $E_{\text{ave}}$ ) in the drift region between the anode and cathode was thus more than 3.3MV/cm. For the 30  $\mu\text{m}$   $L_{\text{AC}}$  SBD, a reference device without the NiO RESURF structure only achieved a BV of 2.8kV.

Leakage current at 10kV reverse bias was  $2 \times 10^{-6}\text{A}/\text{mm}$ , ten times lower than reported for gallium nitride SBDs.

A 17  $\mu\text{m}$   $L_{\text{AC}}$  device had more than 8kV BV, corresponding to an  $E_{\text{ave}}$  of 4.7MV/cm. The BV reduced to 6.1kV at 200°C, giving 3.6MV/cm  $E_{\text{ave}}$ .



**Figure 2. Benchmarks of team's device ("This work") against competition: (a) differential specific on-resistance ( $R_{\text{on,sp}}$ ) versus BV for reported Ga<sub>2</sub>O<sub>3</sub> SBDs, p-n diodes, and transistors with BV more than 3kV. (b) The BV versus maximum operational temperature for reported high-temperature Ga<sub>2</sub>O<sub>3</sub> SBDs, p-n diodes, and transistors with BV more than 100V. Dotted line shows approximate boundary of prior data. Arrow shows desirable target. Note that 10kV BV of higher-BV device reflects measurement limit rather than actual BV.**

The researchers comment: "The BV's negative temperature coefficient ( $\eta_T$ ) suggests the lack of avalanche breakdown and implies a trap-assisted breakdown mechanism." The team points out that the achieved range of  $E_{\text{ave}}$  exceeds the critical fields for GaN and silicon carbide (SiC). GaN lateral SBDs have been reported with  $\sim 1\text{MV}/\text{cm}$   $E_{\text{ave}}$  and 10kV BV.

The RESURF structure had a negative impact on (differential)  $R_{\text{on,r}}$ , increasing it by about a factor of 2, relative to Ga<sub>2</sub>O<sub>3</sub> SBDs without RESURF.

The Baliga figure of merit (FOM,  $\text{BV}^2/R_{\text{on}}$ ), which balances the effect of breakdown and forward current flow, is improved for the RESURF devices by a factor of more than 5, compared with reference SBDs without.

Electrical parameters, such as turn-on voltage ( $V_{\text{on}}$ ), Schottky barrier height, and ideality factor, were similar for all devices, coming in at around 1V, 0.74eV, and 1.2, respectively.

Increasing the operating temperature to 200°C almost doubled  $R_{\text{on,r}}$  while  $V_{\text{on}}$  reduced to 0.7V. The on/off ratio was more than  $10^6$ , even at 200°C.

The researchers present benchmarks of the BV and  $R_{\text{on,sp}}$ /maximum operation temperature (Figure 2). The researchers comment: "The Baliga's FOM of 17  $\mu\text{m}$ - $L_{\text{AC}}$  devices is 906MW/cm<sub>AC</sub> at 25°C. The FOM of the 200°C-operational, 10kV-class device ( $L_{\text{AC}} = 30\mu\text{m}$ ) is at least 370MW/cm<sup>2</sup> at 25°C (the true FOM is expected to be much higher due to BV > 10kV)." ■

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