

Flexible indium phosphide DHBT frequency boost

A wafer-scale process has resulted in record performance for flexible electronics.

Southeast University and Nanjing Electronic Devices Institute in China have claimed the first demonstration of wafer-scale fabrication of high-frequency indium phosphide (InP) double heterostructure bipolar transistors (DHBTs) transferred to a flexible substrate [LiShu Wu et al, *Semicond. Sci. Technol.*, vol36, p03LT02, 2021].

The team reports: "The cut-off frequency $f_T = 337\text{GHz}$ and maximum oscillation frequency $f_{MAX} = 485\text{GHz}$ are obtained, which represents the highest result ever reported in the field of flexible electronics to date."

Flexible electronics is deployed in areas such as displays, solar cells, wearable electronics and bio-medical devices. Existing flexible electronics suffers from limited frequency performance, below the speed and bandwidth needed to access wireless communications/Internet of Things (IoT) technology. InP-based technology allows access to higher frequencies through much higher electron mobility.

Although new technologies such as graphene have enabled f_T values of 198GHz ($28.2\text{GHz } f_{MAX}$), the best flexible electronics performance previously was also achieved with InP, using high-electron-mobility transistor structures, achieving $160\text{GHz } f_T$ and $290\text{GHz } f_{MAX}$.

The researchers contrast their wafer-scale achievement with previous reports, none of which "have yet been demonstrated to achieve high-performance flexible electronics at multi-gigahertz range on wafer scale, which will also limit the abroad application of RF flexible electronics."

The DHBT material was grown on 3-inch InP substrate using molecular beam epitaxy (MBE) — see Figure 1. The material was fabricated into single-finger DHBTs, using a $0.5\mu\text{m}$ process. Wet etching was used to define three stacked mesas for the DHBT,

Emitter contact	InGaAs	200nm	Si
Emitter	InP	200nm	Si
Base	InGaAs	35nm	C
Set-back	InGaAs	30nm	Si
δ -doping	InP	50nm	Si
Collector	InP	150nm	Si
Collector contact	InGaAs	50nm	Si
Sub-collector	InP	200nm	Si
Etch-stop	InGaAs	100nm	Undoped
Substrate	InP		Semi-insulating

Figure 1. Layer structure of the InGaAs/InP DHBT.

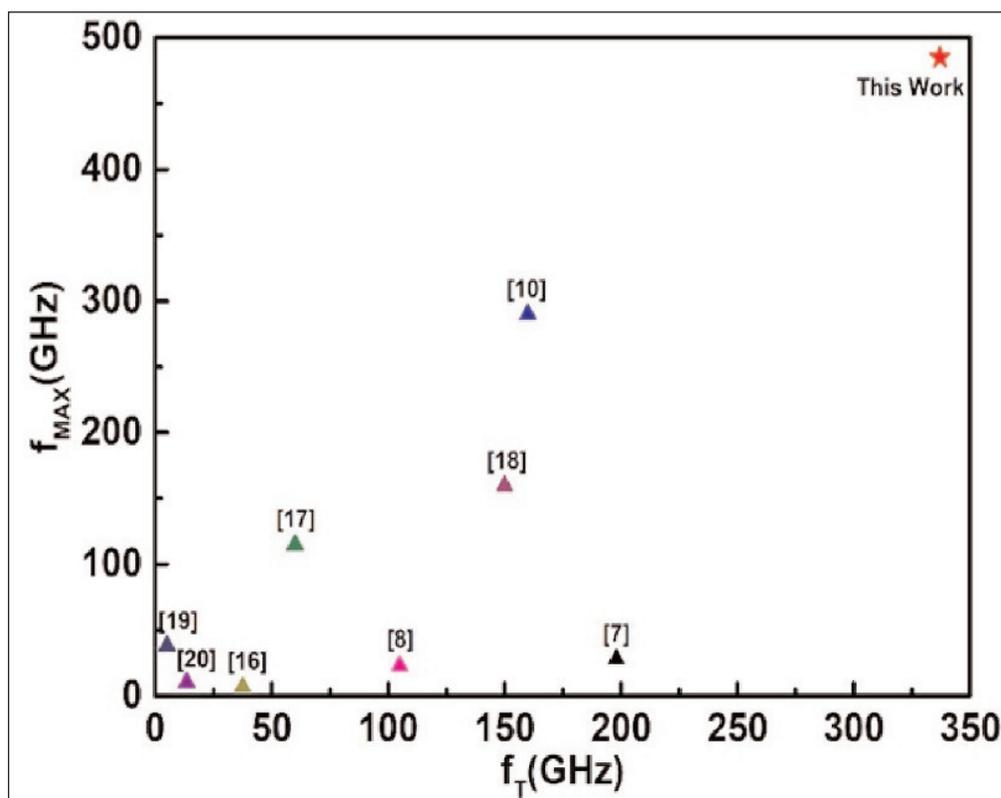


Figure 2. Comparison of f_T/f_{MAX} with previously reported semiconductor transistors on flexible substrate.

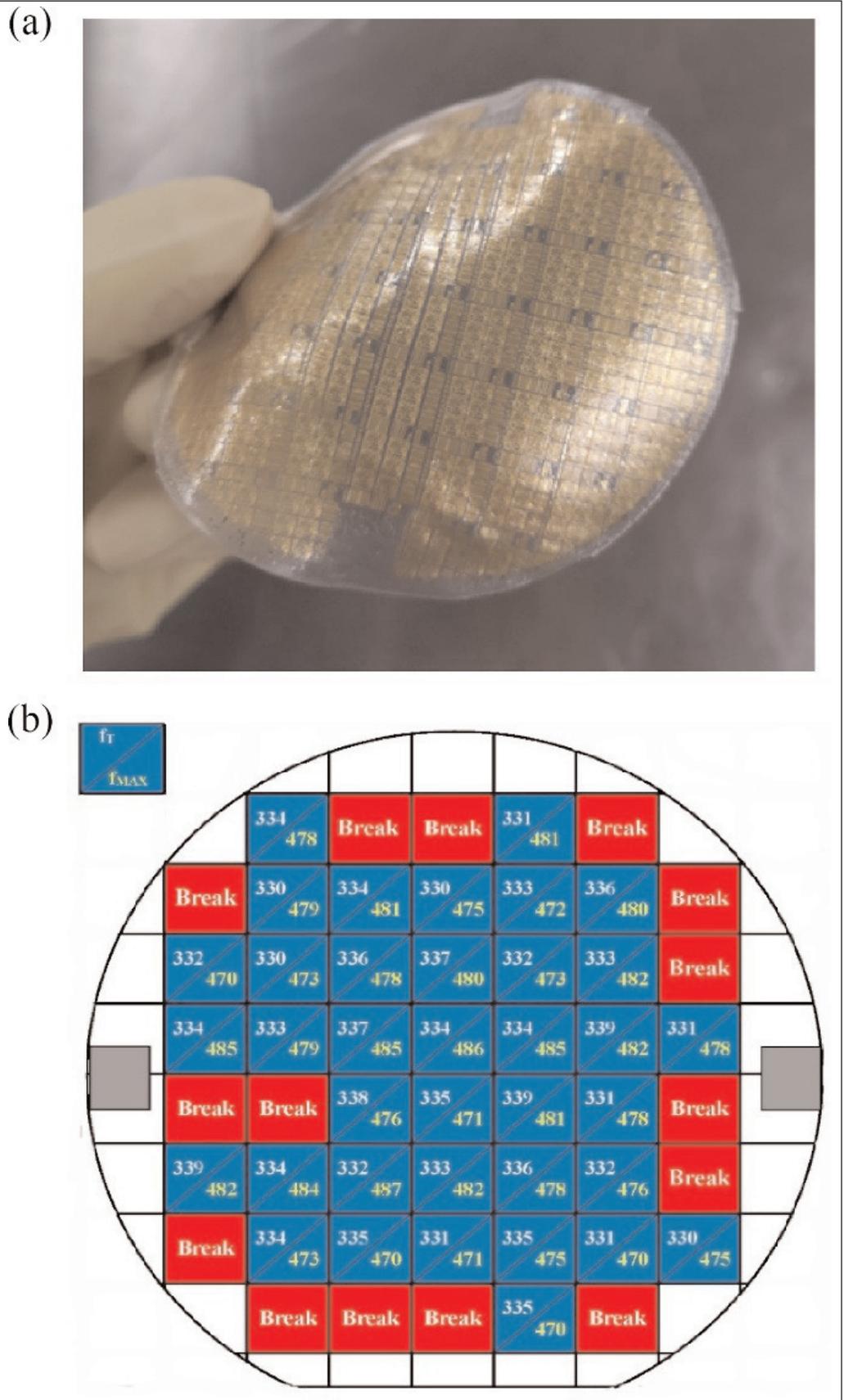
Figure 3. (a) Optical image of 3-inch InP DHBTs on flexible substrate. (b) f_T/f_{MAX} performance mapping under same measurement condition.

using self-aligned techniques to define the base contact. The emitter/collector metals were titanium/platinum/gold, and the base was platinum/titanium/platinum/gold. Further steps included device isolation, planarization/passivation with benzocyclobutene, reactive-ion etch to expose metal terminal posts, and pad deposition.

The transfer to flexible substrate involved temporary adhesion to sapphire carrier to enable removal/thinning of the InP substrate using mechanical lapping, followed by selective wet etching with a solution based on hydrochloric acid. The indium gallium arsenide (InGaAs) stop layer was removed with a solution based on orthophosphoric acid. The 2 μm -thick device was then permanently bonded to the flexible substrate, and the sapphire carrier was removed.

DC measurements showed some degradation in performance in terms of collector current relative to devices not transferred to flexible substrates. The researchers attribute the degradation to poor thermal conductivity of the flexible substrate, about a factor of three lower than for InP. Self-heating can severely impact transistor performance. The maximum gain of 31 was only slightly impaired relative to the non-flexible devices.

The frequency performance was measured up to 40GHz. A conventional DHBT achieved an extrapolated f_T of 385GHz with an f_{MAX} of 570GHz. The DHBT on flexible substrate registered an f_T of 337GHz and an f_{MAX} of 485GHz. The researcher compared their work with other reports (Figure 2).



The process yield was around 73%, with most failed devices being on the periphery of the wafer (Figure 3). The failure was attributed to local defects. The frequency performance of the resulting devices varied only slightly. ■ <https://doi.org/10.1088/1361-6641/abe05b>
Author: Mike Cooke