High-breakdown normally-off gallium oxide transistors

Researchers claim record for β-Ga_2O_3 MOSFETs on silicon substrate.

Saudi Arabia's King Abdullah University of Science and Technology (KAUST) has claimed record breakdown voltages for normally-off beta-phase gallium oxide (β-Ga_2O_3) metal-oxide field-effect transistors (MOSFETs) on gallium nitride (GaN) on silicon substrate [Mritunjay Kumar et al, Appl. Phys. Lett., p126, p193505, 2025].

The reported maximum reverse-bias breakdown was measured at 540V, the highest among previously reported studies on breakdown voltage of β-Ga_2O_3 MOSFETs on silicon substrates, according to the KAUST team. The β-Ga_2O_3 material is presently in the laboratory phase of its device development, and the ultimate breakdown capability enabled by the 4.9eV ultrawide bandgap is presumably some way off. This bandgap should be able to sustain electric fields up to 8MV/cm. Commercial advanced power handling materials include GaN and silicon carbide (SiC) with wide bandgaps up to 3.4eV.

The researchers comment: "Despite advancements in β-Ga_2O_3 thin-film growth technology via various growth methods on heterogeneous substrates, there is no demonstration of β-Ga_2O_3 power MOSFETs utilizing GaN buffer-on-Si substrates."

The use of low-cost, commercially available GaN/Si substrates is seen as being "significant for high performance and their monolithic integration with GaN devices in future power integrated circuits". In particular, more thermally conductive GaN on Si could ease the temperature management problems of β-Ga_2O_3. Other options for thermally conductive substrates include SiC, but these substrates are very costly.

In addition to power handling, the KAUST team suggests that the combination with GaN could enable β-Ga_2O_3 radio frequency devices for power switching and RF amplification systems.

The researchers explain: "Given β-Ga_2O_3's higher breakdown voltage compared to GaN, it complements GaN's superior mobility. This allows high-speed control circuitry to be implemented with GaN technology, while high-power devices are realized using β-Ga_2O_3, leveraging both technologies to develop monolithic power-integrated circuits (ICs)."

The researchers used an economical and scalable β-Ga_2O_3 growth technique: pulsed laser deposition (PLD).

TFTs (Figure 1) were fabricated on 50nm β-Ga_2O_3 layers on 4.7μm GaN on p-Si(111) substrates. The β-Ga_2O_3 was doped with silicon to give an n-type electron majority carrier character. The semi-insulating GaN buffer contained a carbon doping concentration of $5x10^{19}/cm^3$.

The β-Ga_2O_3 layers were grown by 700°C PLD with a 102mJ/pulse laser ablating Ga at 5Hz in an environment with oxygen at 5mTorr partial pressure. The electron transport properties gave $1.2x10^{18}/cm^3$ electron concentration and $2.06cm^2$/V-s mobility from Hall-effect measurements.

The researchers comment: "The relatively low bulk mobility of the epitaxial β-Ga_2O_3 film is primarily due to its polycrystalline nature, and lattice-mismatch-induced defects from growth on GaN/Si substrates."

The team suggest that mobility could be enhanced by deploying metal-organic chemical vapor deposition (MOCVD) growth rather than PLD. With post-deposition annealing this would increase crystallinity and decrease defect density.

The surface roughness of the β-Ga_2O_3 was 0.57nm, doubling the 0.23nm of the underlying GaN substrate, according to atomic force microscopy (AFM) on a

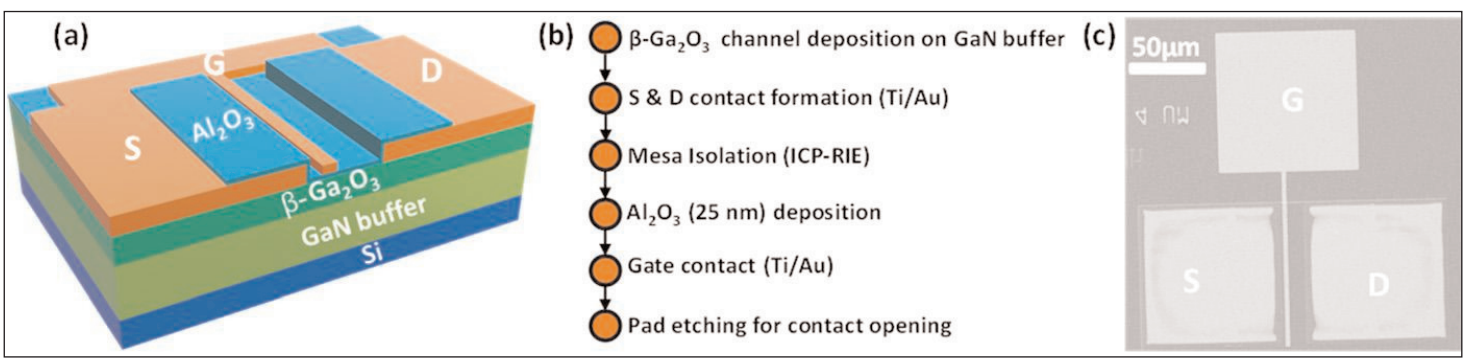

Figure 1. β-Ga_2O_3 TFT device structure: (a) three-dimensional (3D) schematic, (b) process flow, (c) scanning electron microscope (SEM) image.

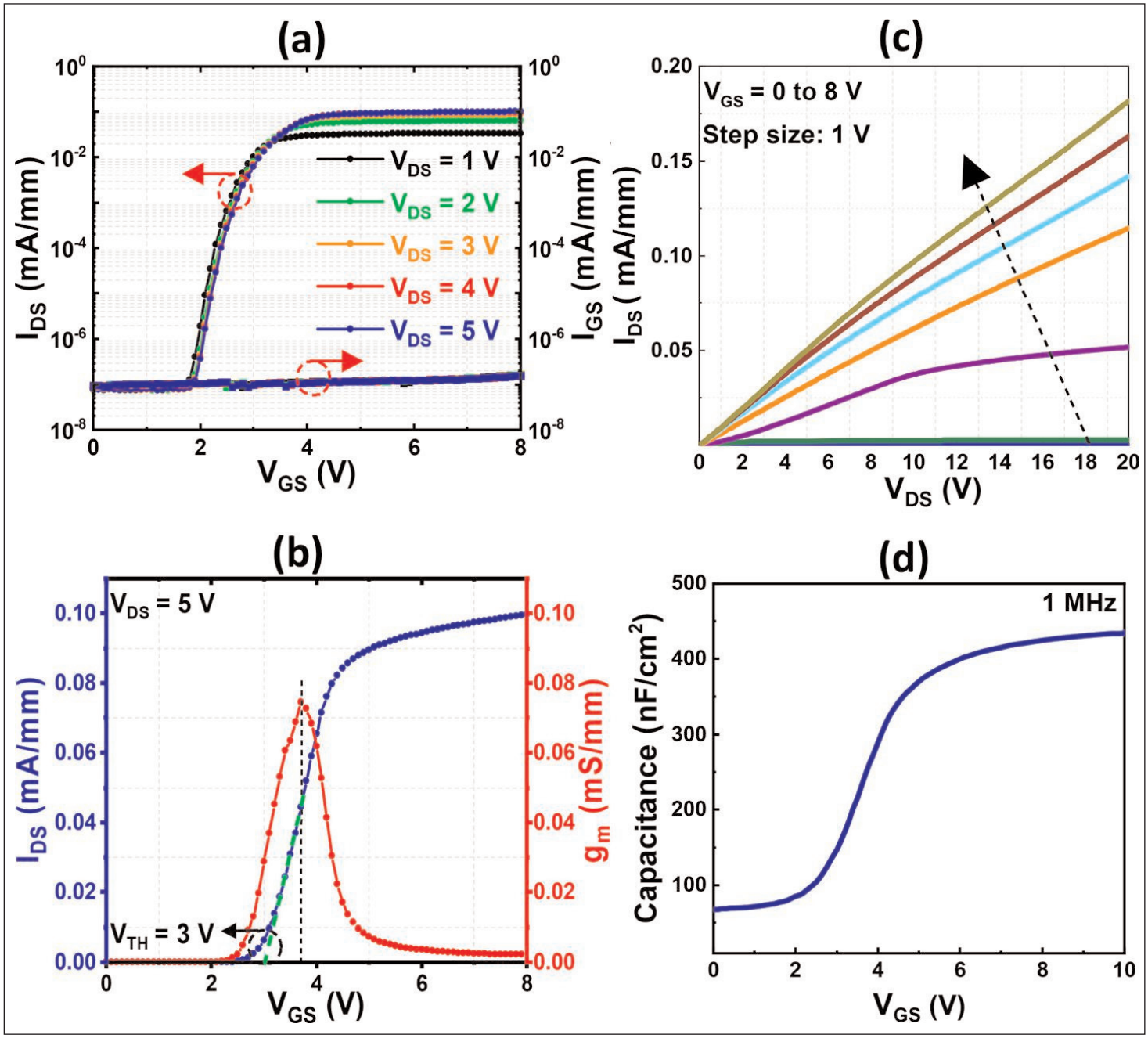

Figure 2. Electrical characteristics: (a) current-gate voltage transfer (I_{DS}–V_{GS}) at different V_{DS}, (b) V_{TH} calculation by linear extrapolation at transconductance (g_m) maximum, (c) output characteristics at different V_{GS}, (d) capacitance–voltage (C–V) measurement at 1MHz.

5μmx5μm field.

The source/drain (S/D) electrodes of the TFTs consisted of titanium/gold (Ti/Au). The gate (G) structure consisted of 25nm aluminium oxide (Al_2O_3) dielectric and Ti/Au electrodes. The gate length (L_g) was 4μm; and, the S (L_{SG}) and D (L_{GD}) distances to the gate were 3μm and 18μm, respectively.

The TFTs demonstrated a low 167mV/decade sub-threshold swing (SS) and high 10^6 on/off current ratio (Figure 2). The team comments: "The low SS for the fabricated device indicates a high-quality interface between β-Ga_2O_3 and Al_2O_3."

The interface trap density (D_{it}) was estimated to be $4x10^{12}$/cm^2-eV, using capacitance–voltage measurements.

The Al_2O_3 dielectric enabled a small gate leakage of order 10_7mA/mm at 8V forward gate potential. The transistor threshold was at +3V at 5V V_{DS}, giving enhancement-mode (normally-off) behavior. Such behavior is favored for fail-safe power system operation.

The researchers comment: "The positive V_{TH} of β-Ga_2O_3 MOSFETs is contributed by both the top-side and bottom-side depletion, along with possible phase-induced insulating regions near the β-Ga_2O_3/GaN interface."

The team reports that the threshold point can be controlled by the β-Ga_2O_3 layer thickness.

A field-effect mobility of 1cm^2/V-s was extracted from transconductance measurement, using a transistor

Table 1. Electrical parameter comparison of reported β-Ga_2O_3 TFTs on heterogeneous substrate. KAUST work in bold.

Material preparation method	Substrate	V_{TH} (V)/operation mode	R_{on} (kΩ-mm)	I_{on}/I_{off}	V_{br} (V)
MOCVD	Sapphire	D-mode		$>10^7$	390
MOCVD	Sapphire	D-mode		10^{11}	400
MOCVD	AlN/Si	−2.17	0.177	10^8	178
PLD	GaN/Si	3	13.6	10^6	540
Exfoliation	SiO_2/Si	−7.3		$>10^6$	344
Exfoliation	SiO_2/Si	7	0.013	10^{10}	185
Ion-cutting	Al_2O_3/Si	D-mode	3	10^6	522
Ion-cutting	Al_2O_3/SiC	D-mode	0.101	10^7	1000
Fusion bonding	β-Ga_2O_3/4H-SiC	−50	0.065	108	2000

with a 30μm-long, 150μm-wide gate at 0.1V drain bias. The maximum drain current was 0.18mA/mm at 8V gate potential, and 20V drain bias. The on-resistance (R_{on}) was estimated to be 13.6kΩ-mm in the linear region.

The researchers also compare their work with other reported attempts to fabricate β-Ga_2O_3 TFTs on various heterogeneous substrates by various methods (Table 1). ■

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