Smart stacking III-V on crystal silicon solar cells to boost conversion

Palladium nanoparticle array connection enables thin-film on aluminium backsurface-field silicon tandem devices to reach 25% efficiency.

apan's National Institute of Advanced Industrial Science and Technology has used palladium nanoparticle (Pd NP) arrays to connect crystalline silicon (c-Si) and III-V tandem solar cell stacks, resulting in high conversion efficiency [Hidenori Mizuno et al, Appl. Phys. Express, vol10, p072301, 2017]. The researchers term the technique 'smart stack'.

While silicon solar cell technology offers the advantages of mature mass production and low cost, single-cell silicon devices are theoretically limited to conversion efficiencies less than ~29%. Using tandem structures with III-V thin-film subcells above c-Si cells could extend this performance.

The researchers used a simple aluminium back sur-

based on a 400µm-thick





double-side mirror polished, p-type Si (100) substrate. An n⁺-Si surface layer was created using thermal diffusion of phosphoryl chloride (POCl₃). The p⁺-Si BSF was achieved through screenprinting and firing of aluminium paste.

The structure was prepared for smart-stack bonding with the indium gallium phosphide/gallium arsenide (InGaP/GaAs) (0.35µm/0.5µm) thin-film cell by creating a Pd NP array in a self-assembled polystyreneblock-poly(2-vinylpyridine) template. The gap between the GaAs and silicon layers was found to be uniformly around 10nm.

The InGaP and GaAs absorber layer thicknesses were designed to give relatively matched currents for the

three subcells from AM1.5g standard solar illumination - 10.7mA/cm² from InGaP, 10.7mA/cm² from GaAs, and 10.2mA/cm² from Si. Matching currents is very important for high efficiency.

The completed structure (Figure 1) included a gold-germanium-nickel (AuGeNi) front electrode plus a silicon dioxide/titanium dioxide (SiO_2/TiO_2) anti-reflective coating (ARC).

The researchers comment: "It should be emphasized that no additional heat treatment was necessary to improve the bonding guality (lower the interfacial resistance), which is usually required with other bondingbased fabrication of two-terminal tandem cells."

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PV measurements with AM1.5g solar spectrum illumination (1 sun, 100mW/cm²) showed 24.5% conversion efficiency n (Figure 2). The researchers found that the open-circuit voltage (V_{oc}) was down on what was expected from measurements on separate cells: "This could be attributed to the shading of the c-Si bottom subcell because, in this situation, unfavorable migrations of photo-generated carriers to unilluminated regions could easily occur. This would lead to an increased dark current ability, and thereby a decreased V_{oc}."



increased dark current Figure 2. Current density-voltage (J–V) characteristics of as-fabricated (beforeand recombination probability, and thereby a cells.

The high fill factor (FF) of 0.827 was attributed to the low resistance interface between the silicon and GaAs given by the Pd NP array.

To improve the performance by tackling the shading issue, the researchers used a dicing saw to remove excess regions of the c-Si bottom cell. This increased V_{oc} , although it reduced the short-circuit current density (J_{sc}) somewhat. The researchers say that the current degradation was not significant — indeed, the FF increased to 0.830 and the conversion efficiency was enhanced to 25.1%. The team adds that the improved performance after using the dicing saw strongly sup-

ports "the hypothesis that smart stack cells are durable enough to withstand rather severe semiconductor processes".

The researchers say that they consider the observed performance as being close to the best achievable for the types of subcells used. "Higher-efficiency smart stack cells will require development of high-quality, thicker InGaP/GaAs cells, advanced c-Si cells, and tricks for current matching between them, which is actively underway in our group," the team adds. **https://doi.org/10.7567/APEX.10.072301** *Author: Mike Cooke*

