Indium gallium nitride light-emitting diodes on thin industry-spec silicon

Researchers find ways to tackle bowing and threading dislocation trade-offs.

esearchers in Singapore and USA have been developing ways to grow III-nitride structures on SEMI-spec 200mm-diameter silicon by metal-organic chemical vapor deposition (MOCVD) [Li Zhang et al. Semicond. Sci. Technol., vol32, p065001, 2017].

Ordinarily such structures are grown on relatively thick silicon wafers (1–1.5mm) to avoid breakage in wafer handling caused by hidden stress in indium aluminium gallium nitride (InAlGaN) layers from lattice mismatch and high-temperature growth and cooling processes. Unfortunately, 200mm silicon wafer manufacturing facilities are based on tools designed to meet specifications of the Semiconductor Equipment and Materials International (SEMI) industry organization, which specifies 725 μ m (0.725mm) thicknesses or thinner.

The Singapore-MIT Alliance for Research and Technology, the National University of Singapore, and the Massachusetts Institute of Technology (MIT) see the work as part of their efforts towards "integration of GaN and Si CMOS as the driver for GaN-on-Si materials and device development". GaN materials are being used and developed for both high-power, high-voltage and high-frequency electronics, along with the longerterm light-emitting (LED) and laser diode applications.

The team used MOCVD equipment with a specially shaped pocket susceptor. A flat susceptor suffers from uneven heating of the substrate. With concave bowing caused by stress, the contact is made in the center of the wafer, giving higher temperatures there. With convex bowing, the temperature is higher toward the edge. The researchers designed a concave pocket with 12 400µm-high protrusions placed radially at 30° separation so that the substrate was suspended above the susceptor, giving more even heating. Bowing of the wafer, if excessive, can cause plastic deformation of the substrate, increasing fragility.

The researchers explain: "By suspending the wafer with 12 protrusions, this design ensures that, during the entire growth run, the wafer is not in contact with the susceptor except at the protrusions. As a result, maintaining a uniform temperature across a SEMI-spec u-GaN 1600 nm SiN_x of different duration u-GaN 400 nm Al_{0.20}Ga_{0.80}N 340 nm Al_{0.40}Ga_{0.60}N 300 nm AlN 210 nm LT-AIN 30 nm

Si (111) substrate (725 μm)

Figure 1. Schematic of optimized epitaxial structure of GaN-on-Si growth for LEDs.

200mm-diameter silicon wafer can be more easily achieved during the entire growth process."

After native oxide removal and pre-treatment of the 200mm-diameter SEMI-spec boron-doped silicon wafer, MOCVD began with 20nm low-temperature (980°C) AIN nucleation.

The temperature was then ramped for 240nm hightemperature AIN, followed by step-graded layers of AIGaN to bridge over to the final GaN layer (Figure 1). The AIGaN layers also introduce compressive strain that was designed to compensate for tensile strain that usually develops when GaN-on-silicon structures are cooled to room temperature.

The AIN initial part of the growth, from tensile strain due to lattice mismatch with silicon, gives a concave

Technology focus: LEDs 71

wafer bow. The AIN to GaN step-grading converts this to convex bowing. The final cooling results in an approximately flat wafer due to differences in the coefficients of thermal expansion of the various layers.

on 0.4µm undoped GaN template on silicon with layer sequence: 2.4µm n-GaN, 3x 1.5nm InGaN/40nm GaN V-pit initiation, 10–15x 2.5nm quantum wells/barriers (MQWs), p-AlGaN electron blocking, and

By suspending the wafer with 12 protrusions, this design ensures that, during the entire growth run, the wafer is not in contact with the susceptor except LED material was grown at the protrusions. As a result, maintaining a uniform temperature across a SEMI-spec 200mm-diameter silicon wafer can be InGaN/10nm GaN multiple more easily achieved during the entire growth process.

p-GaN and p++-GaN for ohmic contact.

V-pits roughen the surface (Figure 2) and give three LED performance advantages. According to the researchers: "The thinner MQWs on the sidewall enhance the efficiency of LEDs in several ways: (i) form a potential barrier to non-radiative recombination; (ii) improve hole injection into the MQWs; (iii) reduce reverse leakage current in the LEDs."

Since the V-pits tend to nucleate on threading dislocations (TDs), the density of V-pits gives an indication of TD density (TDD). For the optimized 450nmwavelength LED structures the V-pit density was 5.5×10^8 /cm². This compares with a minimum V-pit density of 2.7x10⁸/cm² for LEDs produced on thicker (1mm) non-SEMI silicon.

The LEDs on SEMI-spec silicon had an internal quantum efficiency of about 70%. For 300µmx300µm devices, the typical turn-on voltage was 2.5V. Reversed bias leakage was 0.2nA at -4V. Diode ideality was 2.3.

Before producing the LEDs, the researchers worked to optimize the growth processes, in particular step-graded AlGaN structure. A three-step AlGaN layer sequence — 280nm Al_{0.8}Ga_{0.2}N, 300nm Al_{0.4}Ga_{0.6}N, 310nm Al_{0.2}Ga_{0.8}N resulted in minimum concave bow of -4µm. However, the generation of edge-type threading dislocations (TDs), as indicated by x-ray analysis, increases with decreasing Al_{0.2}Ga_{0.8}N layer thickness.

dislocations are more detrimental to device performance and reliability, causing reliability issues in HEMTs [highelectron-mobility tran-

"Generally, edge-type **Edge-type dislocations** are more detrimental... causing reliability issues in HEMTs and increasing non-radiative recombination in the MQWs of LEDs

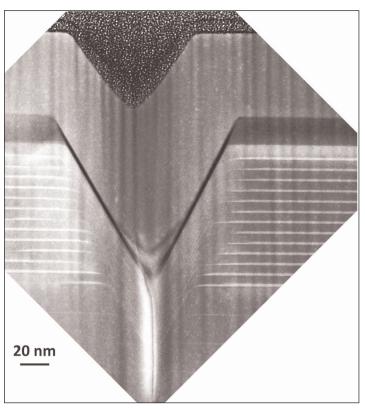


Figure 2. Cross-sectional scanning transmission electron micrograph of V-pit initiation layers and MQWs.

sistors] and increasing non-radiative recombination in the MQWs of LEDs," the team comments. Increasing the Al_{0.2}Ga_{0.8}N layer to 395nm reduced the (102) x-ray peak to 670 arcsec, from 750 arcsec for the minimum bow 310nm layer. However, the wafer bow increased to +72µm convex.

The researchers used a silicon nitride (SiN_x) masking layer in the middle of the u-GaN growth as a technique to balance low bowing with low TDDs. In particular applying silicon nitride on GaN can create a SiGaN₃ monolayer that acts as an anti-surfactant, inhibiting GaN growth. The team comments: "We use the antisurfactant behavior of SiN_x masking to moderate the strain of the subsequently grown GaN layer from the masked GaN layer."

Further GaN growth is from uncovered regions, which reduces dislocation densities. The growth from the uncovered island regions coalesces to form laterally overgrown GaN material. The amount of coverage by SiGaN₃ was controlled by the duration of exposure to disilane (Si₂H₆) and ammonia (NH₃) precursors.

The researchers produced an optimized GaN template for LEDs with a 2-step AlGaN buffer combined with 150-second SiN_x masking that was used for the LED material. A 2-step buffer was found to increase the compensating compressive stress within a thinner layer to counteract bowing.

https://doi.org/10.1088/1361-6641/aa681c Author: Mike Cooke