# Imec presents record $WSe_2$-based 2D-pFETs for extending logic technology roadmap

**Collaboration with TSMC yields $I_{max}$ up to 690μA/μm; partnership with Intel yields improved fab-compatible modules for source/drain contact formation and gate stack integration, with reduced EOT.**

At the 71st IEEE International Electron Devices Meeting (IEDM 2025) in San Francisco, CA, USA (6–10 December), nanoelectronics research center imec of Leuven, Belgium, presented what it claims is breakthrough performance of (with $I_{max}$ as high as 690μA/μm) for p-type FETs with monolayer tungsten diselenide ($WSe_2$) channels, and improved fab-compatible modules for source/drain contact formation and gate stack integration.

These results, achieved through collaborations with leading semiconductor manufacturers, are said to mark a significant advance for 2D-material based technology, which is considered to be a promising long-term option for extending the logic technology roadmap.

Replacing silicon conduction channels with atomically thin layers made of 2D transition-metal dichalcogenides ($MX_2$) promises to enable ultimate gate and channel length scaling, while maintaining good electrostatic channel control and high carrier mobility.

Crucial milestones to be achieved include high-quality 2D-material layer deposition, gate stack integration, low-resistance source/drain contact formation, and 300mm fab integration. Also, while most efforts focus

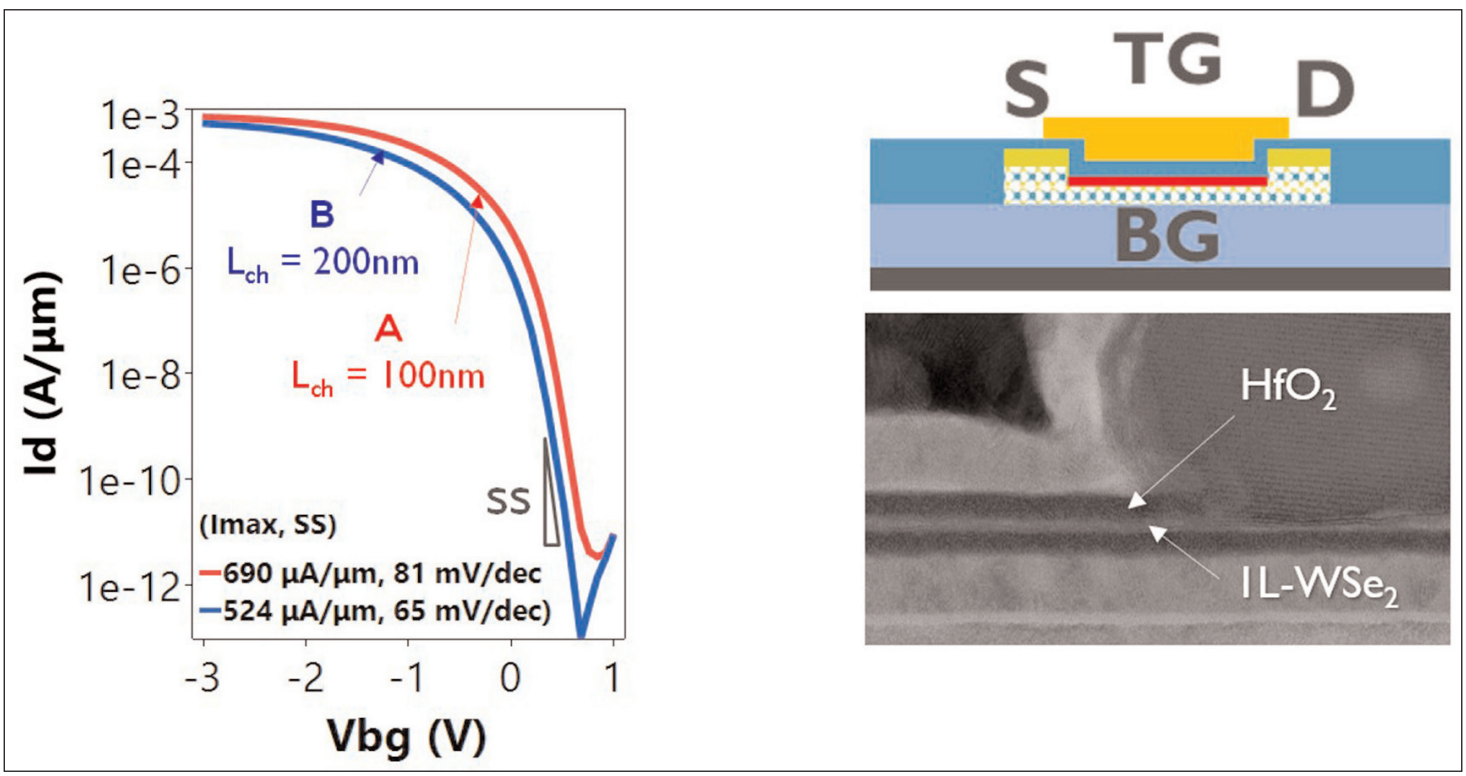


**Figure 1. (Left) Transfer curves of 2D-pFET devices using defect-passivated synthetically created bi-layer $WSe_2$ films, with best device showing $I_{max}$ = 690μA/μm; (right) TEM cross-section of finalized dual-gated 2D pFET ($L_{ch}$=channel length TG=top gate; BG=back gate; S=source; D=drain; IL=interlayer), in collaboration with TSMC.**

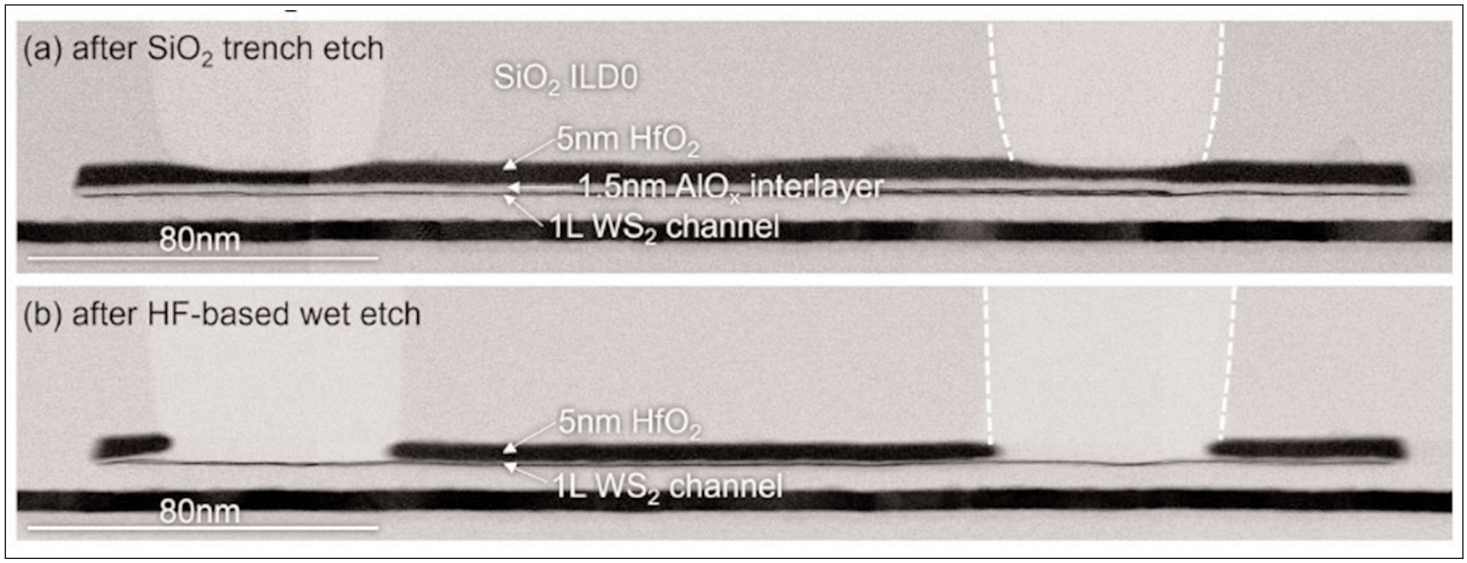


**Figure 2. (a) Trench dry etch into $SiO_2$; (b) dry and wet etch selectively stopping on the monolayer $WS_2$ channel, also causing AlOx interlayer lateral removal along the full channel length (in collaboration with Intel).**

on improving n-type devices (with channels made of $WS_2$ or $MoS_2$), more fundamental work is needed on p-type devices, which require different channel materials (such as $WSe_2$).

"At 2025 IEDM, we show in two separate presentations how in-depth collaborations with leading semiconductor manufacturers within imec's core CMOS Industrial Affiliation Program (IIAP) have enabled breakthroughs in the performance of 2D-material-based devices," says Gouri Sankar Kar, VP R&D compute and memory device technologies at imec. "In both partnerships, combining high-quality 2D material layers provided by the manufacturer with imec's optimized contact and gate modules played a key role in pushing the technology beyond state of the art," he adds.

"Depositing the top-gate $HfO_2$ dielectric on top of a $MX_2$ channel requires an additional seed layer to support $HfO_2$ nucleation and growth," continues Gouri Sankar Kar. "For nFETs, this is solved by creating an AlOx interfacial layer, but this approach is challenging for pFETs due to the different characteristics of the $WSe_2$ channel material as compared to its n-type counterparts."

"In partnership with TSMC, we started with a synthetic bilayer of $WSe_2$, which was formed by subsequently transferring two high-quality $WSe_2$ monolayers from TSMC on our substrates. We then oxidized the top $WSe_2$ monolayer, converting it into an interfacial layer that successfully supported the deposition of the $HfO_2$ gate oxide. This fab-compatible lab-based integration approach resulted in record performance of our dual-gated pFETs."

Another presentation highlights the collaboration between imec and Intel in developing 300mm-manufacturable modules for source/drain contacts and gate stack integration, for n-type ($WS_2$ and $MoS_2$) and p-type ($WSe_2$) 2D-FETs. "The key innovation consists in applying a selective oxide etch process on Intel's high-quality 2D material layers, that were capped with an interfacial $AlO_x$ layer, a $HfO_2$ layer and a $SiO_2$ layer," says Gouri Sankar Kar. "The oxide etch process allowed the formation of fab-compatible damascene-style top contacts — a world first," he claims. "In addition, during the vertical contact etch process, the interfacial $AlO_2$ layer was simultaneously etched laterally, removing $AlO_2$ from the channel region. This significantly lowered the top gate's EOT [equivalent oxide thickness], benefitting the gate's transfer characteristics."

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