# Transcending frequency and integration limits

**Dr Mike Cooke reports on how indium phosphide enables higher-frequency transistors and large-scale integration of optical communication components.**

A wide range of microwave and optoelectronic devices and integrated circuits of such devices can be fabricated on indium phosphide substrates. These devices offer a number of performance improvements over analogous structures fabricated in gallium arsenide.

For example, indium phosphide metal–semiconductor field effect transistors (MESFETs) can take advantage of the higher mean and peak saturation velocities for electrons in InP to boost the cut-off frequency ($f_T$) over GaAs-based devices. However, this is not the route taken these days for improved performance.

The high-electron mobility transistor (HEMT), also known as the modulation-doped FET (MODFET), gives an improvement of about 30% in $f_T$ over the corresponding MESFET. The epitaxial layers making up the traditional HEMT are lattice matched, but, for GaAs, advantages can be gained by using near-lattice-matched (pseudomorphic) or even unmatched (metamorphic) HEMT layer configurations.

Metamorphic layers give a wider range of material choices. InP HEMTs and GaAs metamorphic HEMTs (MHEMTs) have similar frequency performance in terms of low-noise in the range from 10GHz to almost 160GHz, but the MHEMT has better power handling capabilities from about 20GHz to 100GHz. Cutting across this power performance is the gallium nitride HEMT, with a smaller frequency range (possibly up to 60GHz by 2011), but much higher power densities.

One of the main drawbacks of working with InP is the brittle nature of the substrate. While leading-edge silicon substrates are 300mm (12 inch) in diameter, InP is currently limited to 100mm (4 inch) with 75mm (3 inch) more common, mainly because of its fragility, compared to diameters for GaAs (which is stronger than InP, but more brittle than Si) of up to 150mm (6 inch). University researchers commonly work with specialists rather than producing InP devices in-house, perhaps an indication of the difficulty of working with the material. In 2002, Japan's Showa Denko produced 150mm InP monocrystal mirror wafers (semi-insulating), seeing a

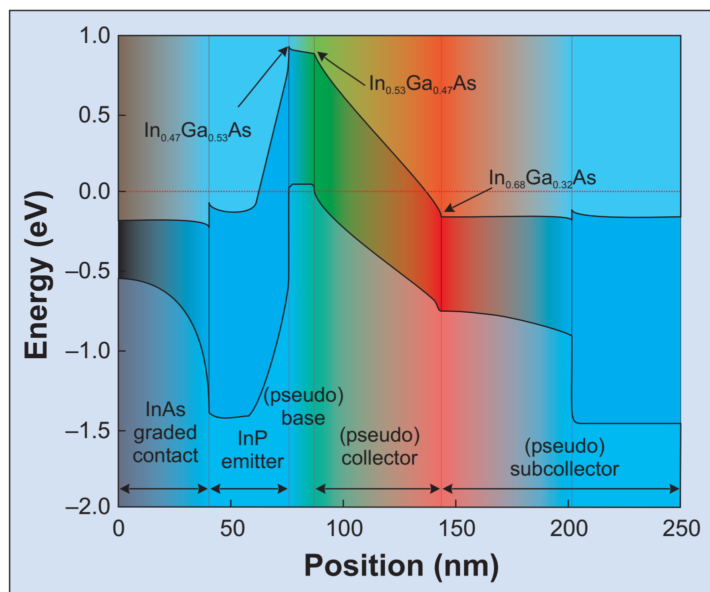


**Figure 1. Energy band diagram for UIUC's 710GHz pseudomorphic HBT.**

"rapidly growing" market for dense wavelength division multiplexing (DWDM) systems. InP-based LEDs, laser diodes and photo-diodes can be produced fitting the optimum wavelengths for optical communication fiber. However, as the company was speaking, the previously manic, "rapidly growing" market was going into a deep depression. But, as will be seen below, there is again some promising activity in this sector. First, we look at the heterojunction bipolar transistor (HBT) structure.

## Bringing pseudomorphism to speed

One research centre that has been pushing InP to the limit is the University of Illinois at Urbana-Champaign (UIUC). The UIUC team has several times held the record for the fastest transistor in recent years. The last such announcement came in 2005 with a 12.5nm-base pseudomorphic HBT with unity current-gain ($f_T$) and power-gain ($f_{max}$) cut-offs of 710GHz and 340GHz, respectively (Hafez et al, Appl. Phys. Lett. **87**, 252109, 2005). The collector current density was 20mA/μm$^2$. A lower current density of 7.5mA/μm$^2$ enabled the device to achieve a higher power-gain cut-off at the expense of $f_T$ ($f_T$ = 540GHz, $f_{max}$ = 407GHz). Higher $f_{max}$ is advantageous in high-speed analog circuit design. HBTs also have potential for the highest-speed digital and mixed-signal circuits with clock rates beyond 100GHz.

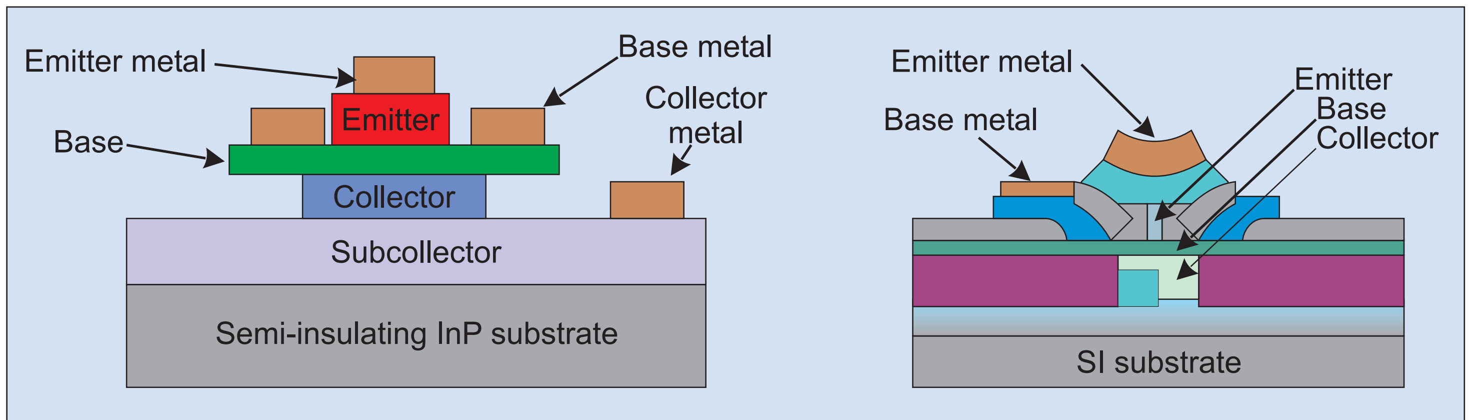


**Figure 2. Conventional mesa InP HBT (left) and DARPA/TFAST's proposed scalable structure (right).**

The latest UIUC results used pseudomorphic structures to overcome limitations of previous work on single (SHBT) and double (DHBT) heterojunction bipolar transistors. For example, SHBTs can achieve an $f_T$ of 550GHz at 20mA/μm$^2$ (Hafez and Feng, IEDM 2004, pp549–552). But it is estimated that vertically scaling the SHBT to achieve terahertz frequencies would require current densities of more than 100mA/μm$^2$ with junction temperatures exceeding 500°C. The pseudomorphic grading of the collector in UIUC's latest device (see Figure 1) enabled reduced current densities and hence lower junction temperatures. By grading the indium content from a lattice-matched $In_{0.53}Ga_{0.47}As$ at the base to $In_{0.68}Ga_{0.32}As$ at the subcollector, the researchers estimate that a 25% increase in electron velocity is achieved over that for a lattice-matched collector. The reason for the improvement is given as being due to increased overshoot distances and mobility in the graded collector. The base is also graded and is very thin (12.5nm).

Other InP advantages for HBTs include a very low surface recombination rate, higher electron mobility compared with GaAs and Si, and a higher drift velocity in the collector at high field, allowing a higher collector breakdown voltage. UIUC has worked with a number of companies in developing its InP devices, such as Vitesse and Epiworks. The latter was founded by two UIUC graduates in 1997.

## Defensive moves

The US military is one of the keenest users of high-performance/challenging technology, including InP devices. Among the US government's 2007 budget estimates for defense research (February 2006) is a Defense Advanced Research Programs Agency (DARPA) project for InP HBTs (Figure 2). 'Technology for Frequency Agile Digitally Synthesized Transmitters' (TFAST) intends to produce mixed-signal circuits that are 'highly integrated' (up to 20,000 transistors, a 10-fold increase on previous technology) operating at beyond 100GHz, along with direct digital frequency synthesizers (DDS) operating at clock speeds up to 30GHz. The estimated budgets for the financial years 2005–2007 are $19.6m, $14m and $10m, respectively. Process technologies are to be developed with feature sizes of less than 0.25μm. The program has been running since 2002 and has involved organizations such as BAE Systems, Vitesse, HRL Laboratories, Lucent Technologies, the Mayo Foundation, Rockwell Scientific and Northrup Grumman Space Technology (Velocium).

TFAST pinpoints the Achilles Heel of InP technology compared with the competing silicon germanium HBT. Despite having helped BAE Systems and UIUC designers to achieve a 152GHz static frequency divider milestone for TFAST in 2004, Vitesse comments: "process yield limitations will prevent increased integration of these submicron-sized devices" (**www.vitesse.com**). Meanwhile the fastest SiGe HBTs have hit 500GHz (R. Krithivasan et al., IEEE Electron Device Letters **27**, 567–569, July 2006), according to measurements made at the Georgia Institute of Technology on an IBM prototype fourth-generation device. SiGe transistors suffer from SiGe's lower electron mobility.

Feedback Linearized Amplifier for RF Electronics (FLARE) is a DARPA project that started this July that plans to follow-up TFAST by developing and using InP HBTs for a wide range of applications such as radar, communication, and electronic warfare systems (e.g. communications jamming). Phase I of FLARE will first design and fabricate InP HBT-based feedback linearized amplifiers to demonstrate the program concept with a dramatic 100-fold improvement in the output third-order intercept point (OIP3) performance parameter without power or noise penalty. In warfare, increased RF spectrum utilization/crowding from friendly or hostile signal interference creates the need for higher dynamic range RF front-ends without compromising system sensitivity (noise figure). Furthermore, many applications and/or

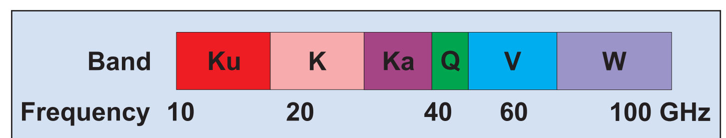


**Figure 3. Microwave bands 10–100GHz.**

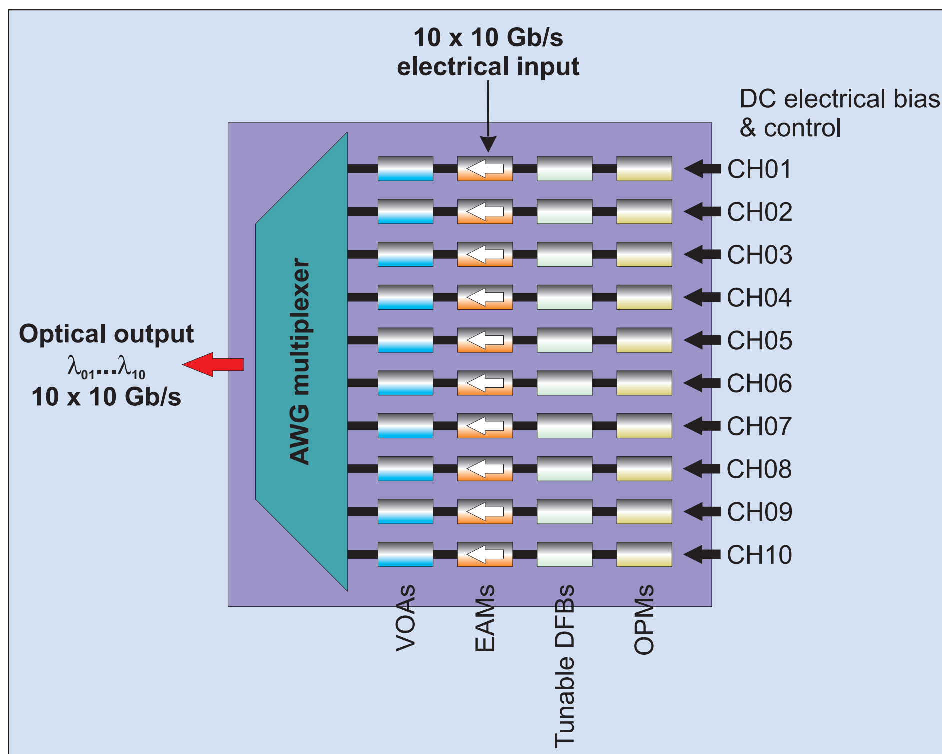


**Figure 4. Infinera's 100Gb/s DWDM large-scale PIC transmitter. The chip incorporates an arrayed waveguide grating (AWG) multiplexer, variable optical attenuator (VOA), electro-absorption modulator (EAM), distributed feedback laser (DFB) and optical power monitoring functions.**

systems are sensitive to power consumption, as in the case of phased arrays, which can include hundreds of front-end microwave amplifiers per array. Phase I also includes concurrent development of 400+GHz InP HEMTs with multi-layer interconnects and advanced low-noise InP HBTs to establish technologies for ultra-high-linearity ultra-low-noise amplifiers (LNA) in subsequent phases. Phase II will extend the Phase I circuit designs by also employing InP HEMTs for ultra-low-noise high-linearity amplifier stages, and will develop manufacturable advanced InP HBTs processes for ultra-high linearity LNA stages. Phase III will then demonstrate:

(1) a composite broadband LNA module consisting of an ultra-low-noise HEMT LNA and an ultra-high-linearity HBT LNA; and

(2) an all-HBT monolithic ultra-high-linearity broadband LNA.

The budget for the first year of this project (2007) is currently $5m, with Rockwell Scientific signed up as 'performer' and University of California Santa Barbara and Vitesse as sub-contractors.

Other DARPA programs developing InP capabilities are Bio-Fabrication (B-FAB), Advanced Microsystems Technology (AMTP), 3-D Microelectromagnetic RF Systems (3-D MERFS), and Scalable MMW Architectures for Reconfigurable Transceivers (SMART) programs.

SMART has the largest projected budget for 2007 ($7.5m) and "seeks to exploit recent advances in analog transmit and receive technology with progress in ultra-high-speed logic to simultaneously reduce the transceiver phase noise and reduce analog device nonlinearities with digital correction techniques," based on SiGe and InP bipolar technologies with speeds in excess of 350GHz.

The 3-D MERFS effort (2007 budget $4m) aims to develop complete millimeter wave (MMW) active arrays on a single or a very small number of wafers, using commercially developed technology. Among recent advances that the project hopes to exploit are InP and SiGe developments that "may allow an entire MMW Electronically Scanned Array (ESA) to become very highly integrated on a sandwich of wafers". This would take advantage of the higher frequencies of the Ka- and W-bands (Figure 3) to put active transmit/receive chips and control circuits on one layer, radiators on another, and a feed system on a third. "This would enable the development of new MMW ESAs of a 6 inch diameter or less for seekers, communication arrays for point-to-point communications, sensors for smart munitions, robotics and small remotely piloted vehicles."

The AMTP project's projected 2007 budget is $5m, but this project has silicon as its main focus, with a subtopic being the creation of technologies for bonding silicon-on-insulator circuits to InP detectors. Finally, B-FAB (2007 budget $2m) is developing biochemical processing of semiconductor devices. InP-based optoelectronics is among the research goals.

## Large-scale optoelectronic integration

InP technology saw a flurry of activity in speculation early in the millennium, before the collapse of the optical-fiber infrastructure market in 2000–2001. With the recent pick-up in optical communications, there has come a modest revival in InP prospects in this sphere. The optimal optical-fiber wavelengths in terms of absorption is 1550nm and for dispersion, 1310nm. There is also a local absorption minimum near 850nm. The bandgap of InP is direct and has an energy of the order of 1.41eV, corresponding to photons of wavelengths around 880nm. Further, it can be lattice matched to $In_{1-x}Ga_xAs_yP_{1-y}$ to access bandgaps down to 0.8eV with a wavelength of 1550nm.

Some companies have decided that this is not where they want to play and have passed their existing interests on to someone else. For example, TriQuint completed the sale of its optoelectronics operations in

Pennsylvania and Mexico to CyOptics in mid-2005. Now TriQuint concentrates on GaAs products. Meanwhile, CyOptics manufacturing facilities now include an InP wafer fab with six in-house MOCVD reactors for wafer growth and regrowth to support internal product requirements as well as offering foundry services. Its packaging, assembly and test facility is automated and is said to be "nanotech capable". Automation is an important step forward in a sector where hand-wiring with the aid of a microscope has previously been the norm. CyOptics says that its core capabilities are in design and production of high-performance photonic chips such as laser diodes (LDs), detectors and avalanche photodiodes (APDs) and in integration and miniaturization of optical engine packaged modules for coarse (CWDM) and dense (DWDM) wavelength division multiplex telecoms systems. Products include InGaAlAs and InGaAsP laser diodes (Fabry-Perot and distributed feedback) aimed at the 1550nm and 1310nm infrared optical-fiber bands, broad-area ridge or buried heterostructure (BH) waveguides, electro-absorption modulators (EAMs), integrated laser modulators (EMLs), semiconductor optical amplifiers (SOAs), multiplexers/demultiplexers, super luminescence diodes (SLEDs), PIN photodiodes, high-speed devices (40Gb/s), and high-power eye-safe lasers. CyOptics also offers GaAs-based laser diodes.

Another InP enthusiast is Infinera, which claims to be able to fit all the key photonic functions found in a typical optical transport system — including lasers, modulators, wavelength multiplexers and demultiplexers, and photodetectors — onto a pair of chips (Figure 4). These are capable of transmitting and receiving more than 100Gb/s of data over long spans of optical fiber, the company says. Its 'photonic integrated circuits' (PICs) currently combine dozens of functions, but Infinera expects eventually to pack 'hundreds'. InP was chosen as the common materials platform as being "the most reliable and cost-effective means of implementing large-scale integration". The company promotes monolithic integration over hybrid integration. 'Hybrid integration' describes the packing of a number of discrete devices in a common module using wire bond or waveguide intra-package connections. 'Monolithic integration' consists of building all the required devices and functions simultaneously on a single substrate, eliminating external inter-device connections. This greatly simplifies manufacturing processes, device separation, assembly, burn-in, testing, and reliability (Figure 5), says Infinera.

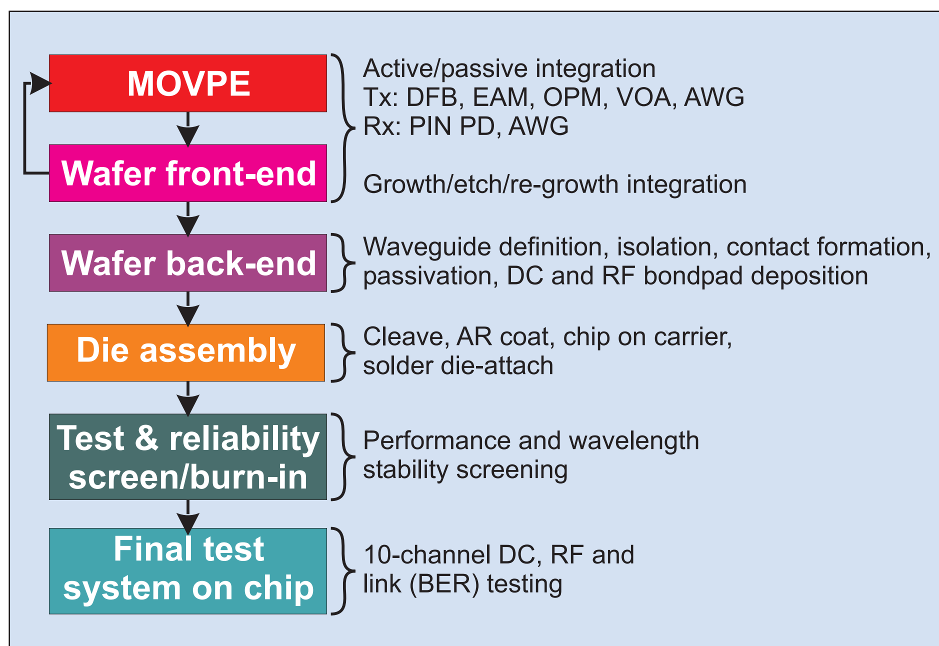


**Figure 5. Process flow for photonic integrated circuit devices.**

The company has selected InP due to its ability to integrate both passive and active optical functions. Silica and/or silicon materials cannot handle the high speeds of more than 10Gb/s aimed at long-haul, regional, metro WDM systems, SONET/SDH, Gigabit per second Passive Optical Networks (PON), Fiber-to-the-Premise (FTTP), and next-generation data protocols such as 100Gb/s Ethernet.

Infinera researchers have written papers on demonstrations of its technology. Nagarajan et al (Selected Topics in Quantum Electronics, **11** (1), 50–65, January/February 2005) describe demonstration of 100Gb/s DWDM transmitter and receiver PICs. The transmitter integrated more than 50 discrete functions onto a single monolithic InP chip. The resultant PICs simultaneously transmitted and received ten wavelengths at 10Gb/s on a DWDM wavelength grid. Later, shorter papers describe the capabilities of a 40Gb/s x 10 = 400Gb/s transmit/receive system (Electronics Letters, **41** (6), 347–349, 17 March 2005) and temperature stability over the range 25–80°C for 10Gb/s x 10 chips (Electronics Letters, **41** (10), 612–613, 12 May 2005).

## Conclusion

While InP has many attractive features as a substrate for electronic and optoelectronics systems, the difficulties involved in processing it mean that, where alternative materials can feasibly be used, they generally are. However, two areas where there are currently no alternatives to InP are transistors operating at the highest speeds (e.g. above 100GHz, especially for defense applications) and large-scale optoelectronic integration (e.g. in photonic integrated circuits) driven by a recovery in the optical communications sector. ■