

Passivating nitride transistors without vacuum processing

Research team claims first application of ultrasonic spray pyrolysis deposition of aluminium oxide in GaN HEMTs.

Researchers in Taiwan have applied a non-vacuum process to deposit aluminium oxide (Al_2O_3) passivation for nitride semiconductor high-electron-mobility transistors (HEMTs) [Bo-Yi Chou et al, IEEE Electron Device Letters, published online 11 July 2014].

Normally, Al_2O_3 is deposited on aluminium gallium nitride (AlGaN) or gallium nitride using vacuum processes such as atomic layer deposition (ALD), metal-organic chemical vapor deposition (MOCVD), or plasma-enhanced chemical vapor deposition (PECVD). The necessity to pump down to vacuum conditions increases process time.

To avoid vacuum processing, researchers at National Cheng Kung University, Feng Chia University, and Industrial Technology Research Institute (ITRI) used ultrasonic spray pyrolysis deposition (USPD) — a technique that has been used for silicon-based solar cell and humidity sensor fabrication, but not previously for GaN HEMTs. The team comments: “The USPD technique possesses advantages of cost-effectiveness, reduced processing time, and non-vacuum environment.”

The researchers used epitaxial material grown on silicon carbide (SiC) using low-pressure MOCVD. The barrier layer was 25nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ and the buffer/channel was $2\mu\text{m}$ GaN.

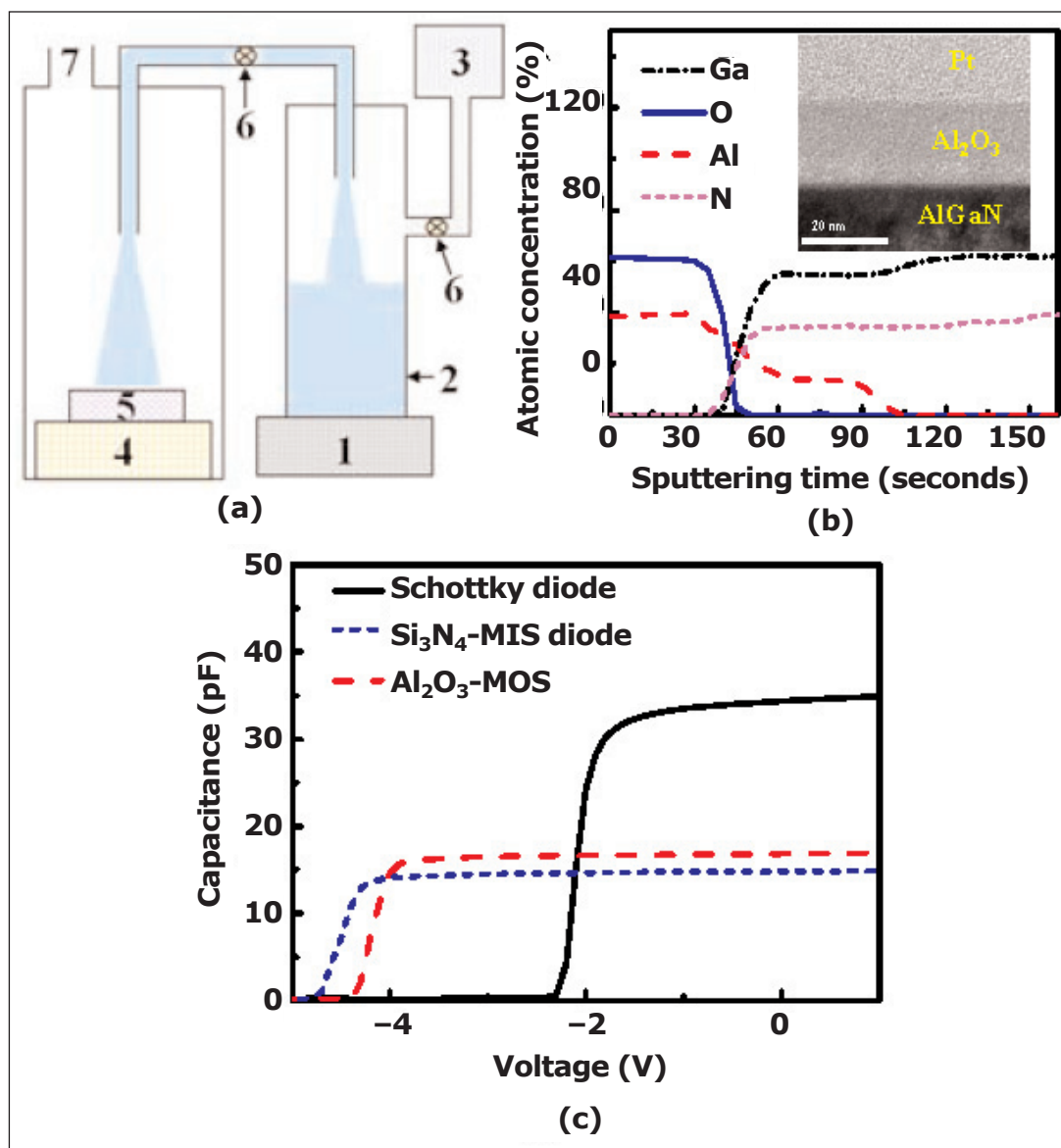


Figure 1. (a) Schematic of USPD system: (1) ultrasonic atomizer, (2) precursor solution, (3) carrier gas supply system, (4) heater, (5) sample holder, (6) controller and (7) exhaust. (b) Atomic concentration of the studied sample by using electron spectroscopy for chemical analysis (ESCA) and, inset, transmission electron microscope (TEM) photo of $\text{Al}_2\text{O}_3/\text{AlGaN}$. (c) C-V characteristics of diodes.

The transistor fabrication involved cleaning, mesa isolation, source/drain contact (Ti/Al/Ni/Au) deposition and annealing, and gate formation and passivation. Three types of device were produced: unpassivated, and passivated with Al_2O_3 or Si_3N_4 . The unpassivated device was annealed at 350°C for six minutes, mimick-

ing the growth condition for the Al_2O_3 passivation. The 100nm Si_3N_4 was applied using 300°C PECVD.

The USPD process (Figure 1) for Al_2O_3 deposition involved aluminium acetylacetonate dissolved in water/ethanol. The precursor was atomized using ultrasound and transported to the 350°C heated substrate in nitrogen carrier gas. At the substrate the aluminium acetylacetonate decomposes to give Al_2O_3 . The resulting layer was 20nm, deposited at the rate 3.5nm/minute. On a 4-inch substrate the thickness uniformity was $\pm 0.7\text{nm}$.

Capacitance-voltage (C-V) measurements on metal-insulator-semiconductor diodes gave dielectric constants of 7.13 and 9.32, respectively, for Si_3N_4 and Al_2O_3 layers.

The corresponding leakage currents under fields of 1MV/cm were $4.8 \times 10^{-6}\text{A/cm}^2$ for Si_3N_4 and $2.2 \times 10^{-8}\text{A/cm}^2$ for Al_2O_3 . The unpassivated Schottky diode structure had a current leakage under reverse bias of $1.5 \times 10^{-6}\text{A/cm}^2$. The areas of the test diodes were $8000\mu\text{m}^2$. The interface trap densities (D_{it}) were estimated at $5.5 \times 10^{11}/\text{cm}^2\text{-eV}$ for Al_2O_3 , compared with $9.7 \times 10^{11}/\text{cm}^2\text{-eV}$ for Si_3N_4 .

Hall measurements (Table 1) showed reduced sheet resistance (RSH) with Al_2O_3 passivation. The improvement is attributed to increased carrier sheet density (n_s) that more than compensates for a slightly reduced electron mobility (μ_n) due to carrier-carrier scattering. The researchers comment: "The obtained higher $n_s\text{-}\mu_n$ product and lower RSH are advantageous to enhance the current drive ability for the present design."

The HEMTs were formed by etching the Al_2O_3 with phosphoric etch. The gate length was $1\mu\text{m}$ and the width was $100\mu\text{m}$. The gate spacing from the source/drain contacts was $2\mu\text{m}$.

A variety of DC, AC and pulsed measurements were made. The researchers comment: "In comparison with unpassivated and Si_3N_4 -passivated devices, reduced D_{it} , decreased leakage current, enhanced drain current

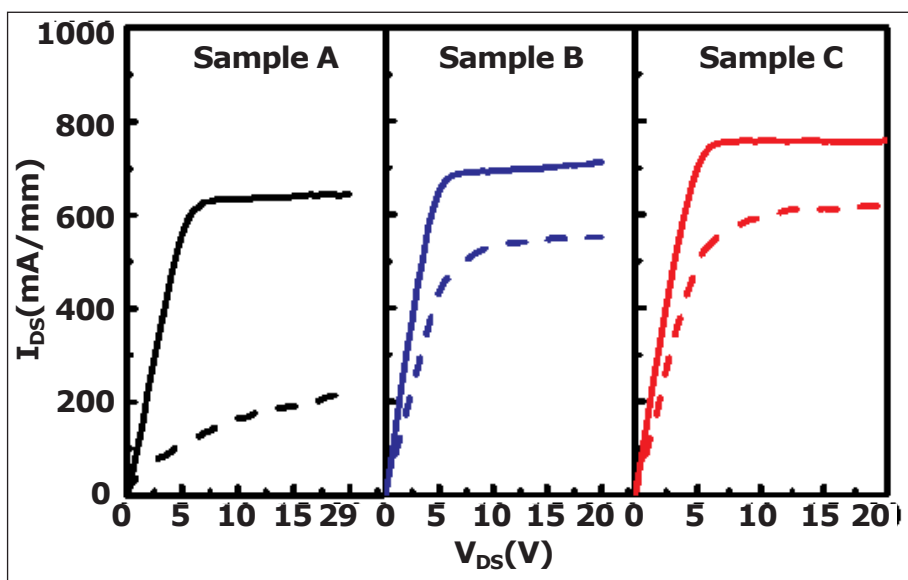


Figure 2. Pulsed drain current-bias ($I_{DS}\text{-}V_{DS}$) characteristics of samples A-C with quiescent-bias points of (V_{DSor}, V_{DS0}) = (0V, 0V) (solid lines) and (10V, -4V) (dash lines).

density, relieved RF drain current collapse, and improved power performance are achieved at the same time for the present Al_2O_3 -passivated HEMT design."

According to the researchers, the reduced current collapse (Figure 2) "indicates that the surface traps in the gate-to-drain/source regions have been effectively suppressed by using the USPD-grown Al_2O_3 passivation layer." ■

<http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6853327>

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Table 1. Hall measurement parameters and DC and AC characteristics.

Sample	A	B	C
Passivation	None	Si_3N_4	Al_2O_3
Hall measurements			
Carrier density	$1.07 \times 10^{13}/\text{cm}^2$	$1.15 \times 10^{13}/\text{cm}^2$	$1.25 \times 10^{13}/\text{cm}^2$
Electron mobility	$1270\text{cm}^2/\text{V-s}$	$1250\text{cm}^2/\text{V-s}$	$1235\text{cm}^2/\text{V-s}$
Sheet resistance	$460\Omega/\text{square}$	$434\Omega/\text{square}$	$404\Omega/\text{square}$
DC measurements			
Maximum drain current	$552.7\text{mA}/\text{mm}$	$629.2\text{mA}/\text{mm}$	$686.6\text{mA}/\text{mm}$
Drain current at 0V gate	$337.6\text{mA}/\text{mm}$	$384.2\text{mA}/\text{mm}$	$421.7\text{mA}/\text{mm}$
On resistance	$10.94\Omega\text{-mm}$	$9.5\Omega\text{-mm}$	$8.65\Omega\text{-mm}$
Source resistance	$2.4\Omega\text{-mm}$	$2.2\Omega\text{-mm}$	$2\Omega\text{-mm}$
Drain resistance	$7.3\Omega\text{-mm}$	$6.3\Omega\text{-mm}$	$5.9\Omega\text{-mm}$
Peak transconductance	$114.1\text{mS}/\text{mm}$	$131.3\text{mS}/\text{mm}$	$152.4\text{mS}/\text{mm}$
Off breakdown for 1mA/mm source-drain current and -6V gate	75V	70V	109V
Gate-drain breakdown for 1mA/mm gate-drain current	-103.8V	-94.5V	-152.4V
2.4GHz measurements at 15V drain bias and -2V gate potential			
Maximum output power	18.5dBm	19.3dBm	20.5dBm
Power added efficiency	25.1%	29.4%	33.6%