Increased maximum oscillation for ETH double-heterostructure transistor

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Researchers at ETH-Zurich have reported increased maximum oscillation frequency for its indium phosphide/gallium arsenide antimonide (InP/GaAsSb) double-heterostructure bipolar transistors (DHBTs) [Rickard Lövblom et al, IEEE Electron Device Letters, published online 12 July 2013].

Based on radio-frequency measurements between 0.2GHz and 40.2GHz, the researchers extrapolated a cut-off frequency (f_T) of 428GHz and a maximum oscillation (f_{MAX}) of 621GHz. "To the best of our knowledge, this represents the highest f_{MAX} reported for any InP/GaAsSb DHBT," the researchers write. The performance beats ETH's previous device by 100GHz for f_{MAX} [reported at www.semiconductor-today.com/news_items/2011/MAY/ETH_020511.html].

The epitaxial material (Figure 1) was grown on 2-inch semi-insulating indium phosphide (InP) substrate using metal-organic chemical vapor phase epitaxy. The InP and GaAsSb have a staggered 'type-II' band alignment where the conduction and valence band offsets are in the same direction at interfaces. The material design had a zero conduction band offset at the base-emitter junction and 150meV offset at the base-collector junction.

The devices were built using a triple mesa process. The emitter contact was 0.3μm wide and the base was 0.5μm. The emitter–base junction width was 0.2μm, giving an emitter area of 0.2μm x 4.4μm. The structure was achieved using electron-beam lithography and a hybrid dry/wet etch.

Layer	Material	Doping	Thickness
Emitter	n-$Ga_{0.25}In_{0.75}As$	Si $3.8x10^{19}/cm^2$	5nm
Grading	n-$Ga_{0.25}In_{0.75}As$ ↑ n-$Ga_{0.47}In_{0.53}As$	Si $3.8x10^{19}/cm^2$	10nm
Emitter	n-$Ga_{0.47}In_{0.53}As$	Si $3.8x10^{19}/cm^2$	
Emitter	n-InP	S $3.0x10^{19}/cm^2$	130nm
Emitter	n-InP	Si $2.5x10^{16}/cm^2$	5nm
Grading	n-InP ↑ n-$Ga_{0.22}In_{0.78}P$	Si $2.5x10^{16}/cm^2$	10nm
Emitter	n-$Ga_{0.22}In_{0.78}P$	Si $2.5x10^{16}/cm^2$	5nm
Graded base	p-$GaAs_{0.59}Sb_{0.41}$ ↑ p-$GaAs_{0.41}Sb_{0.59}$	C $8.4x10^{19}/cm^2$	20nm
Collector	n-InP	S $1.3x10^{17}/cm^2$	125nm
Collector pedestal	n-InP	S $2.2x10^{19}/cm^2$	50nm
Etch stop	n-$Ga_{0.40}In_{0.60}As$	Si $3.0x10^{19}/cm^2$	20nm
Sub-collector	n-InP	S $2.2x10^{19}/cm^2$	300nm
Substrate	InP	Semi-insulating	350μm

Figure 1. Epitaxial layer structure.

The emitter electrode metals were titanium/platinum/gold. The base electrode consisted of platinum/nickel/platinum/gold.

The emitter sidewall and base extrinsic surface were passivated with silicon nitride. Undercut etching was used to reduce the length of the collector mesa with the aim of decreasing the extrinsic base–collector capacitance.

Application of the final metal interconnects was preceded by a low-temperature (less than 190°C) Teflon-based etch-back planarization developed at ETH [see www.semiconductor-today.com/news_items/2012/JULY/ETH_120712.html].

The high f_{MAX} performance was attributed to the small emitter width of 0.2μm and the reduced extrinsic base–collector capacitance. Improvement in f_T over other devices produced by ETH was attributed to "a higher Kirk current density achieved by raising the collector doping level."

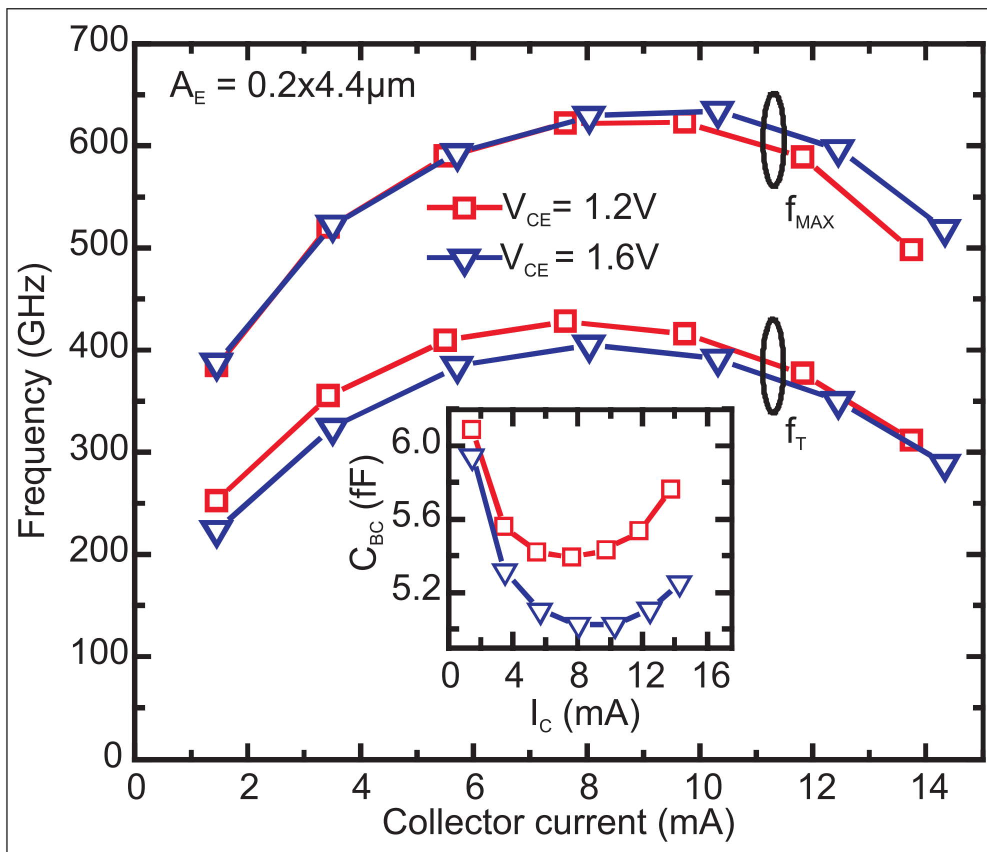

Figure 2. Dependence of f_T and f_{MAX} on collector current at 1.2V and 1.6V collector–emitter biases. Inset: total base–collector capacitance as a function of collector current.

The Kirk effect in bipolar transistors is a significant increase at high current densities of the transit time across the base region, degrading device performance. A higher Kirk current density means a delay in the onset of the effect.

Bias conditions for the quoted frequency cut-offs were 7.6mA collector current and 1.2V between collector and emitter. Varying these conditions (Figure 2) decreased the cut-off frequency but increased f_{MAX} to 634GHz (1.6V collector–emitter). The device's DC peak current gain was 19 and the common–emitter breakdown voltage (BV_{CEO}) was 5V at 1kA/cm^2 collector current density. ■

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