GaN-based HEMT improvement using advanced structures

Giuseppe Vacca gives an overview of the benefits obtainable from innovative gallium nitride transistor architectures.

In order to overcome silicon's performance limitations, the general trend in research has changed to the use of wide-bandgap semiconductors and devices made with innovative structures; in fact, devices built with silicon cannot be improved significantly due to the material's intrinsic limitations.

In recent years, high-electron-mobility transistor (HEMT) devices fabricated from group III-V compound semiconductor materials have been growing rapidly in terms of utilization and proliferation.

This trend applies to both well-established gallium arsenide materials technology (AlGaAs/GaAs) and especially to newer gallium nitride materials technology (AlGaN/GaN).

Indeed, AlGaN/GaN devices seem to be the most promising technology, considering that it can potentially be used to cover a vast array of applications, such as RF and microwave amplifiers with operating frequencies up to the S-band and in many cases working at frequencies of 4GHz and above.

The devices can also be used in the power supply and power management environments, where typical applications are products such as switched-mode power supplies (SMPS), electronic welding units, home appliances, inverter equipment and, in general, AC-to-DC and DC-to-DC converters.

The advantages of GaN are well known: the wide energy bandgap permits a large breakdown voltage, and the higher charges provide higher current; the power density is hence more than 10 times that in GaAs and silicon devices.

In every application GaN shows performance that is at least an order of magnitude greater than that of silicon. It has hence been considered the reference semiconductor for the whole electronics industry over the last few years.

To improve electrical performance together with the reliability that is currently available between the compound semiconductors present on the market, many researchers are studying new transistor structures that enable an increased power level to be managed in these kinds of new devices.

Over the last few years experiments have been performed on new technology consisting of introducing a novel electrode (the field plate) in power HEMT structures designed for radio-frequency, microwave and power applications: this technique has been developed especially for the new AlGaN/GaN heterojunction transistor types.

Due to the integration described, this type of device has already achieved significant improvements and important results regarding electrical performance. Also, very good reliability — of more than 20 years mean time between failure (MTTF) — has been reached.

Additional field-plate integration foresees placement in the median position, between the gate and drain electrodes, in order to enable electric field modulation. In particular, the main function performed by this new electrode is reshaping the electric field distribution profile, spreading it along the device's channel; this is because the maximum electric field is a dominant factor for reliability in high-voltage GaN HEMT transistors.

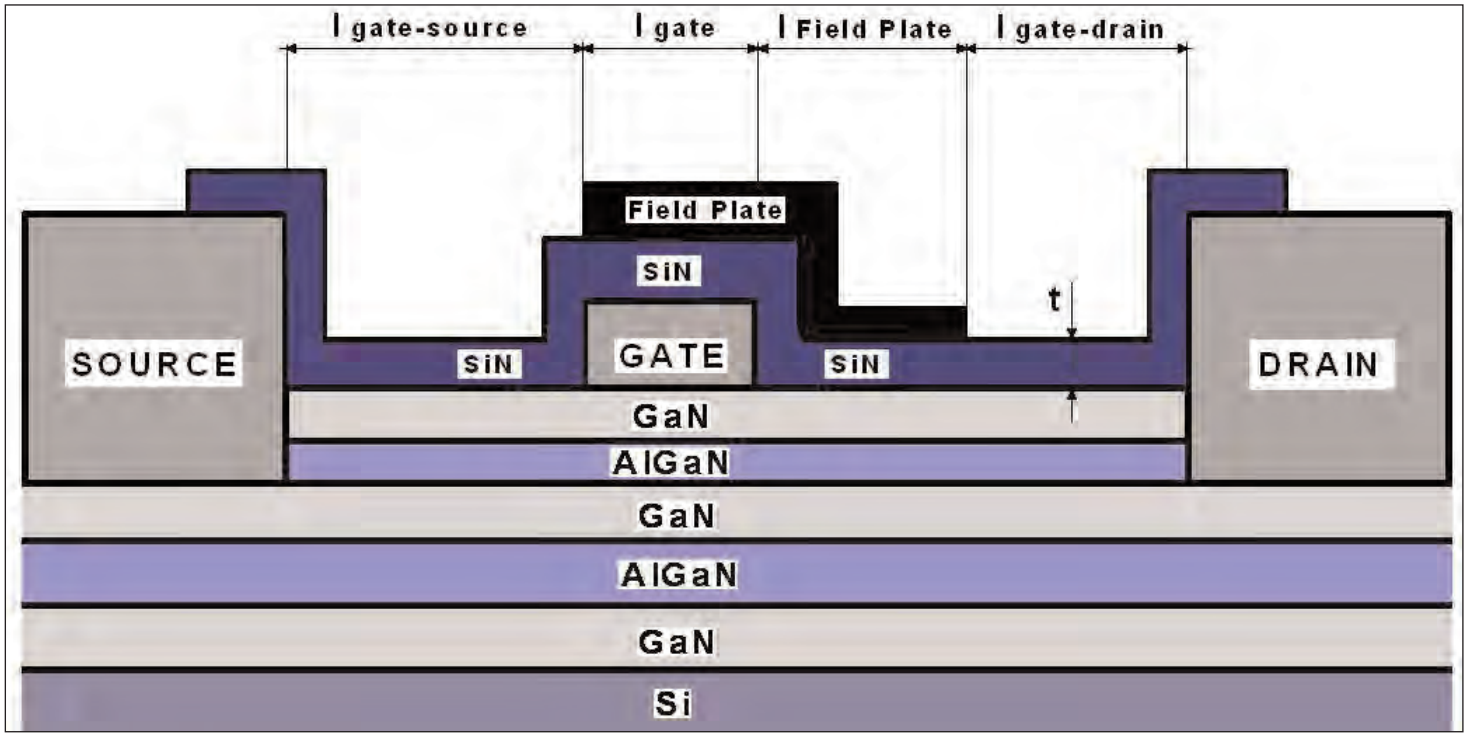
By using a field plate it is possible to achieve a reduction in the maximum peak value of electric field concentration at the drain side of the gate edge. This happens due to the depletion zone formed under the field plate.

The main benefits are a large increase in the breakdown voltage and a reduction in high-field trapping effects in the surface, enhancing current–voltage swings at high frequencies.

Overall, the power density can increase greatly: due to the higher breakdown voltage, in some cases it can grow from 10W/mm to about 40W/mm.

Moreover, the addition of a field plate allows a reduction in the parasitic effect of DC-to-RF dispersion (otherwise termed drain-current collapse). In fact, if the device is affected by this phenomenon, the drain current reached during RF operation is lower than the value obtained in DC mode, so the output power achievable during RF operation is lower and device performance is less than expected.

Experiments have shown a reduction in current collapse, especially for high-voltage applications (compared to the expected value) in devices with field-plate structures, since these help to improve large-signal RF performance compared to devices without a field plate.



AlGaN / GaN HEMT cross section with introduction of field-plate electrode.

Field plates also allows a reduction in the high-frequency dispersion effect in high-power applications.

This new electrode can be fabricated by covering part of a silicon nitride (SiN) passivated layer through an extension of the metallization gate, starting from the gate edge, towards the drain contact.

Field-plate geometry is the key factor to increasing device performance, but correct optimization regarding the plate extension area and the passivated layer is also needed.

A comparison between devices without a field plate versus those equipped with a field-plate electrode can be explained by looking at the electric field distribution. The profile shows the presence of a high single peak placed at the drain edge of the gate contact side; this happens in the case of devices without any field-plate electrode.

If this field plate is present, the shape of the electric field is modified in a novel profile that shows two lower peaks: the first one is located close to the gate (like the previous case); the second one is placed at the edge of the field plate.

Using the field-plate structure it is possible to increase the device breakdown voltage because the new electrode splits the peak of the electric field, relaxing its concentration, and distributes it across the region among the gate and drain: in this way the maximum value of the breakdown voltage rises.

There is a relation between field-plate structure dimensions and breakdown voltage; in particular, the electric field distribution in the channel can be optimized by changing the field-plate electrode geometry because two parameters could be modified: they are the length of the field plate ('Field Plate') and the thickness 't' of the silicon nitride (SiN) dielectric layer.

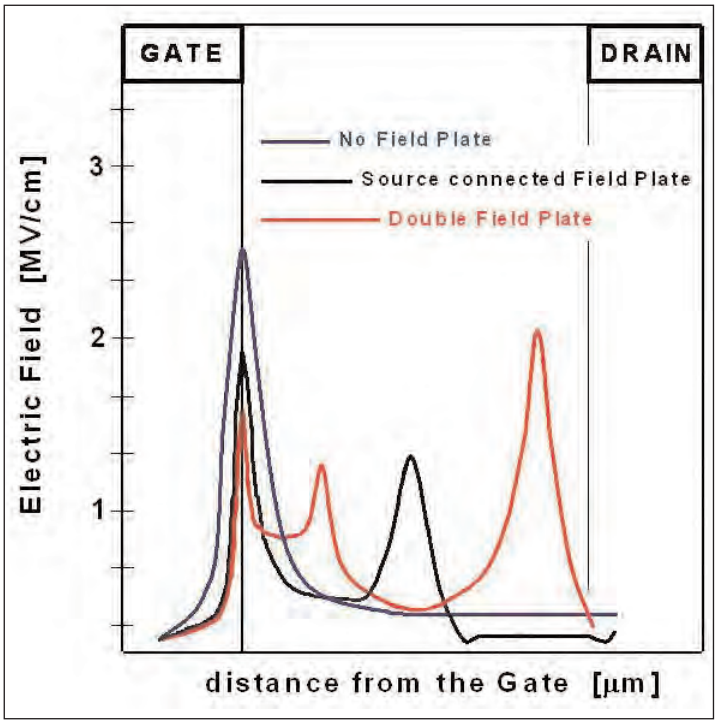
The gate length 'l gate' establishes the transit time under this electrode and the field-plate length determines the size of the reshaping region.

In particular the device's breakdown voltage is enhanced if the field-plate length is increased; this trend is followed up to the saturation point, which changes for different voltage levels. This occurs for different SiN layer thickness 't', and also the breakdown voltage increases with the thickness of this layer up to a defined point. However, above a certain value, there is no further increase in breakdown voltage. So, there is an optimum thickness of the SiN passivated layer that maximizes the device's breakdown voltage.

By performing a transient time gate assessment, it can be seen that FP structures help to recover the drain current and will consequently improve device reliability. A field plate reduces the maximum electric field, and this fact leads to lower electron temperature. In devices without a field plate, hot electrons diffuse into the bulk and are trapped, but if a field plate is used, the electron temperature can be reduced.

The addition of the FP electrode represents an insertion of parasitic capacitance that decreases and limits the behaviour in small-signal conditions.

In order to obtain improvements in the device performance in terms of small-signal conditions together with the breakdown voltage characteristic, other advanced structures have been studied in experiments. One of these consists of the insertion of a double field plate. This kind of structure is built by using essentially two distinct field plates. The first electrode is placed in the gate-drain access region and the second one is connected to the gate terminal.



Electric field profiles from gate to drain.

This technique is quite easy to apply because it is based on standard planar transistor fabrication, and this is an attraction for GaN transistors specifically designed for power-switching applications.

Another kind of advanced structure foresees connection of the field plate to the source. This connection with the FP electrode generally remains joined to the ground.

A double field-plate structure exhibits three peaks in the electric field profile, while devices with the source connected to the field plate have only two peaks. These two peaks in many cases are lower than the three peaks present in devices with two field plates.

Some other types of experimental and non-conventional FP structures have been proposed. One is called 'fingered field plate', and in the simplest case consists of a double FP where small fingers of the FP metal structure (connected with the gate) penetrate into the SiN passivation.

In conventional FP structures, the RF delay propagation time due to gate fingers introduces a phase difference between the gate and the field plate. This can reduce the breakdown voltage and increase the high field trapping; it occurs in particular if the gate finger dimension is comparable to the signal wavelength.

It is possible to solve this issue by using a new, simpler structure obtainable by shorting the FP electrode to the gate at the end of the gate fingers: the metal FP and an exposed metal gate area have to be connected together (using a metal evaporation process) at their ends.

Due to this fix the breakdown voltage still increases. Also, the minimum noise figure and gain are both improved.

The impact caused by the new structure is small since no additional processing is needed to achieve it; it needs just a small change in one photolithography mask.

The dimension, depth and spacing between fingers can be changed in order to optimize the distribution of the electric field. Generally, it is necessary to have 4–5 fingers placed at 1–2μm distance with an extension of 0.2–0.4μm into the passivated layer.

Using a multi-field-plate structure, it is possible to obtain complete control of the shape of the electric field, but with this kind of structure the engineering device processing is quite difficult because multiple connections are required.

A further complication is present in the multi-fingered modulated depth FP: in this case it is very important to optimize the distance downwards of every single finger.

Regarding this structure, a particular biasing level is required for every finger. The first one is drain connected while the last one is generally grounded. The voltage difference between adjacent fingers can be about 100V.

Another non-conventional structure is termed 'Inner Field Plate' because the FP is incorporated between the gate and drain electrodes, at the drain side. Due to this structure it is possible to reduce the gate–drain leakage current, maintaining high-frequency performance. In particular, with this kind of FP the leakage current characteristics depends on the biasing of the inner electrode, V_{IFP}. If the voltage is a negative value (e.g. –15V), the leakage current can be 10–20% smaller than in the case of no biasing (V_{IFP}=0V). The inner FP is promising for high-power microwave applications.

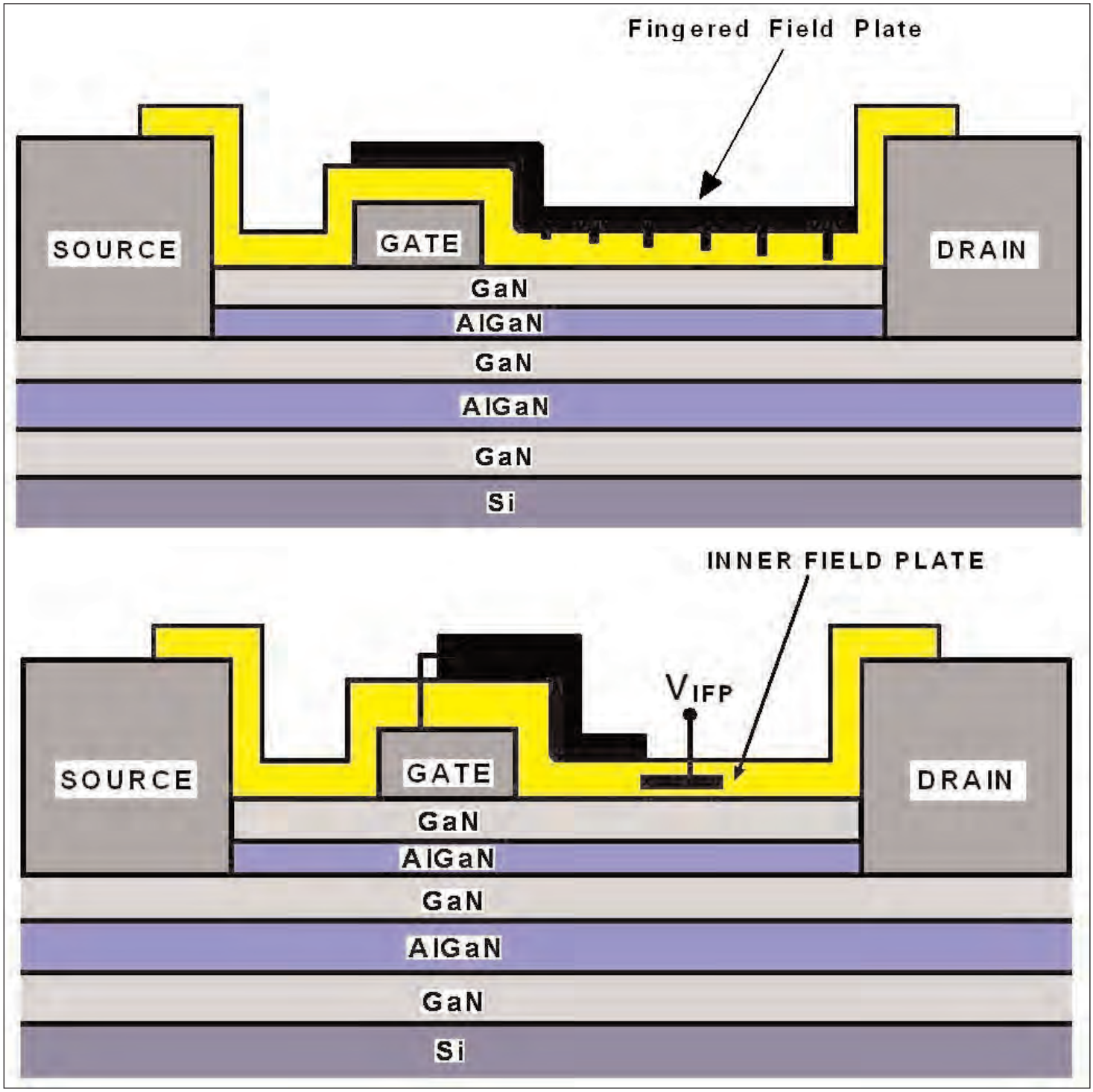
Overall, due to the adoption of field-plate structures, besides reducing the maximum value of electric field, it is possible to improve the control of surface traps that have a bad collateral effect of decreasing the drain current. The impact is particularly marked in situations where the trap concentration is quite high.

Surface traps represent the main cause of GaN HEMT performance degradation when operating at high frequency. Here, field-plate structures reduce trap occupation by limiting the tunnelling injection of electrons into surface traps of the gate-drain region and improve the transient operation of the device.

Also, the leakage current is reduced significantly, by more or less an order of magnitude, assuming the additional field plate. Devices with such a structure show a lower 1/f spectral noise level compared to standard devices.

Although promising good performance, there are some limitations due to parasitic effects and reliability problems (such as superficial and volume traps) that cause a limiting effect on the drain current, particularly related to pulsed conditions.

Defects affecting the gate junction introduce an important reverse leakage current and soft-breakdown problems. A specific study must be dedicated to kinks effects, the consequence of which is the insertion of micro-hysteretic behaviour along the current–voltage characteristic.



AlGaN / GaN HEMT cross sections with (top) fingered modulated-depth field plate and (bottom) inner field plate.

The degradation due to hot electrons under different bias conditions of the device produces stress effects that occur during operation conditions with current collapse.

At the moment the identification of breakdown mechanisms is not clear because there are some scientifically controversial points regarding the determination of the events that occur during the breakdown phenomenon; this factor is quite strong for short-channel devices.

It is necessary to pay attention to studying the correlation between the degradation of GaN HEMT device performances for events related to stress in the continuous regime and at radio-frequency conditions.

In general, technical immaturity will leave space, in future years, for improvements to be achieved, with efforts focused on the geometry of the materials and an in-depth study of the parasitic elements, since the technology has great potential for improvement. ■

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