Millimetre-wave SiGe IC design – a technology overview

Increasing consumer demand for high-data-rate wireless applications has resulted in accelerated development activity to exploit the millimeter-wave frequency range, where large amounts of spectrum are available. The ISM band around 60GHz (V-band) and the light-licensed spectrum at E-band (71–76GHz and 81–86GHz) are both of particular interest. While commercial millimeter-wave ICs have traditionally been realised using III-V based technologies, the increasing availability of SiGe processes with very high f_T values offers an alternative solution that benefits from the potential for lower unit costs in volume production. Stuart Glynn and Liam Devlin of Plextek RF Integration explore in detail the design considerations for exploiting SiGe technology in millimeter-wave applications.

Silicon germanium (SiGe) technology uses heterojunction bipolar transistors (HBTs) to provide impressive transistor performance up to high millimeter-wave frequencies. One of the main features of the SiGe HBT that allows superior performance compared to a silicon bipolar junction transistor (BJT) is a base with a graded germanium (Ge) concentration. The resulting transistors have higher β, higher f_T and f_{max} and lower NF_{min}, making the more advanced SiGe processes potentially suitable for millimeter-wave applications.

A number of vendors now offer on a commercial foundry basis SiGe processes that are suitable for the realisation of circuits operating at V-band and E-band. One such vendor is IHP, a European foundry with a range of high f_T SiGe processes. Figure 1 shows the preparation and processing of SiGe wafers in the IHP pilot line.

While transistors with adequate f_T are a necessary requirement for developing millimeter-wave SiGe ICs, there are many other issues that complicate the design process and must be adequately addressed:

- substrate losses;
- grounding inductance;
- breakdown voltage (which reduces with increasing f_T);
- thermal issues (e.g. self heating, particularly when biased for highest f_T).

This technology overview investigates the realization of analogue circuits for V-band and E-band applications using appropriate IHP SiGe processes. It considers the design of amplifiers as a vehicle for assessing the achievable performance, the implementation issues, and the appropriate design approaches. Process selection, device and bias selection, and the choice of circuit architecture required to demonstrate strong performance at millimetre-wave frequencies, are also considered.

Figure 1: Preparation and processing of SiGe wafers in the IHP pilot line (courtesy R.Weisflog/IHP).

V-band IC design

Process selection: When considering the design of millimeter-wave silicon circuits, it is tempting to select the process with the highest available f_T. However, considerations such as breakdown voltage, cost and current consumption led to the selection of the SG25H3 process for V-band operation. It is a 0.25µm technology, which features high-performance npn HBTs offering a good compromise between breakdown voltage

(BV_{CEO} = 2.3V) and high frequency operation (f_T/f_{max} = 110/180GHz).

Bias point: For peak f_T the current density of high performance npn HBTs on this process is around 6mA/μm^2. However, simulations of G_{max} and NF_{min} at different values of Vbe were carried out, to gauge the bias point that would allow a suitable trade off between gain and noise figure. These plots of G_{max} and NF_{min}, as a function of V_{be}, for a device in common emitter configuration, are shown in Figures 2 and 3. At this stage zero emitter grounding inductance was assumed. A V_{ce} bias of 1.7V was used to optimise linearity. The emitter area is 0.22μm x 6.72μm.

The selected bias point was a collector current density of 3mA/μm^2, corresponding to a typical Vbe of 0.87V, as this offers a good compromise between G_{max} and NF_{min}. The choice of V_{ce} bias of 1.7V was made considering linearity, voltage swing and device breakdown voltage. Under these quiescent conditions, the HBT dissipates 5.1mW/μm^2, which is relatively low, meaning that performance degradation due to thermal issues is less of a concern. This allows an HBT of a given emitter area to be implemented with fewer parallel devices (a lower value of M) and hence with a reduction in the associated interconnect parasitics being introduced in layout.

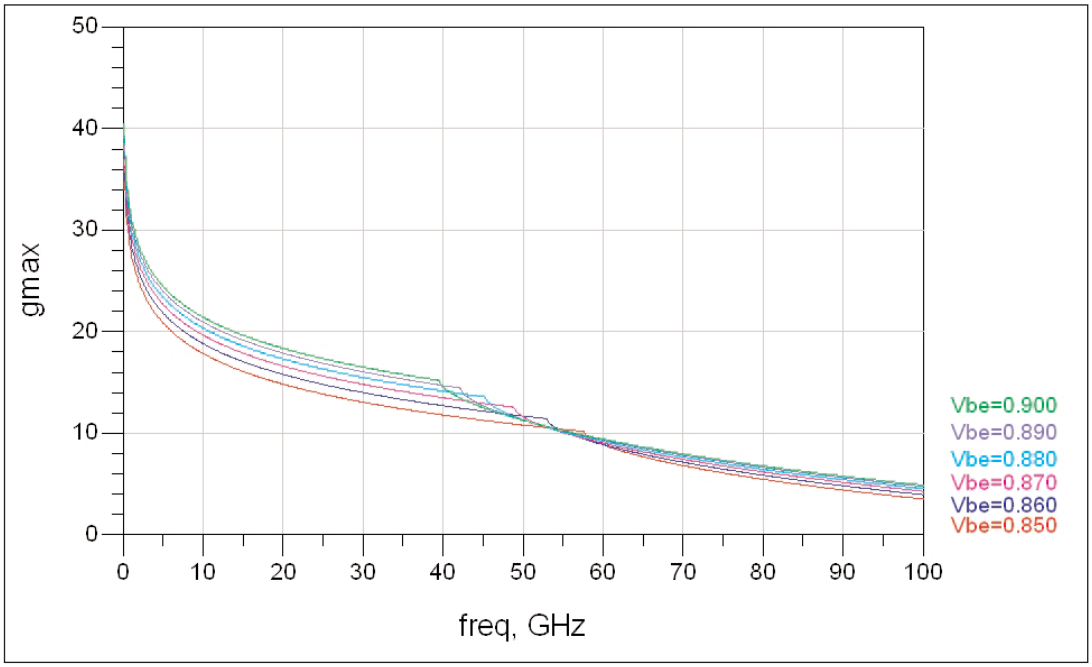

Figure 2: G_{max} versus frequency for different bias points, SG25H3 transistor.

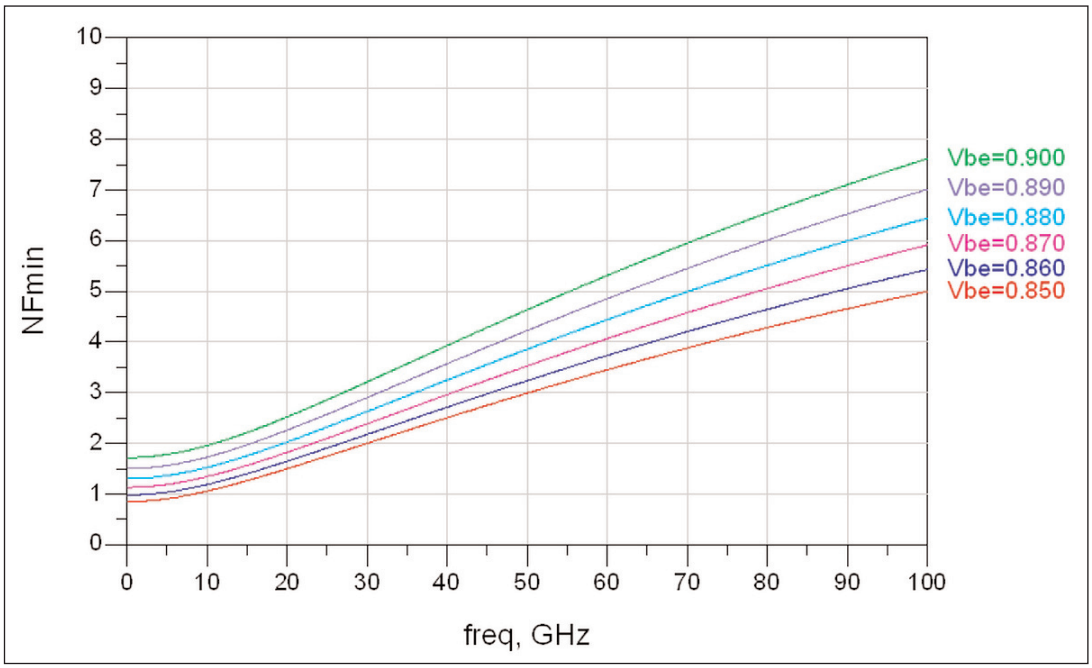

Figure 3: NF_{min} versus frequency for different bias points, SG25H3 transistor.

The selected device in common emitter configuration is unconditionally stable above 49GHz at the chosen bias point. This is evident from the inflection in the G_{max} characteristic at this frequency, showing where the device moves from a region of potential instability to a region of unconditional stability. Being unconditionally stable across the band of interest (57–65GHz) is an attractive feature, as a conditionally stable device would need additional stabilising circuitry, which would cause a drop in gain.

V-band amplifier architecture: Assuming the amplifier is to be used in a real application, then the practical issues of assembly and packaging must be considered from the outset. In particular the expected grounding inductance can be problematic. Regardless of the approach taken to minimise grounding inductance it will still be significant at millimeter-wave frequencies. Overlooking this will result at best in an amplifier with lower gain, and most likely in an unstable amplifier. Interestingly many publications on millimeter-wave SiGe amplifiers ignore this inductance, choosing to only mention performance when measured on a RF-on-wafer (RFOW) probing station, which allows for an effective grounding inductance approaching zero.

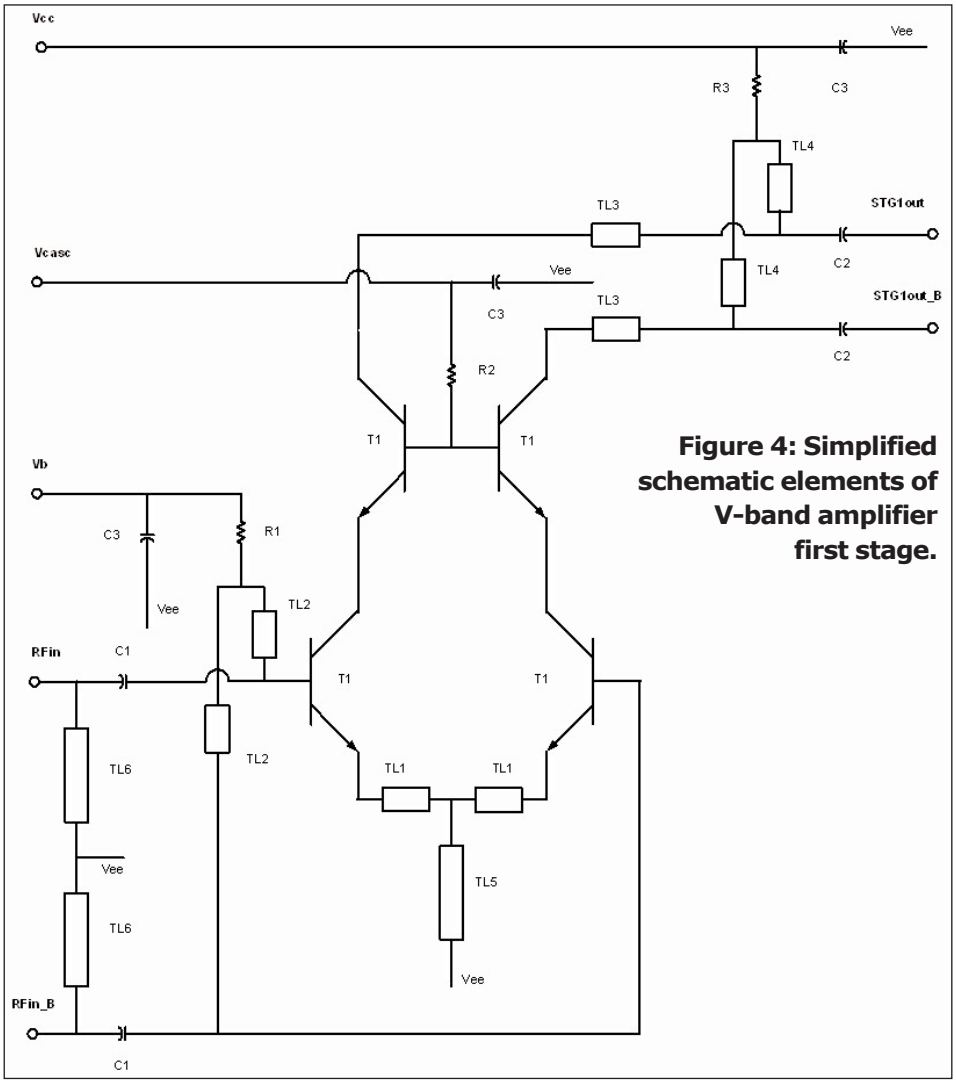

Figure 4: Simplified schematic elements of V-band amplifier first stage.

Packaging and assembly of V-band and E-band ICs is a complex matter in its own right, and a detailed discussion of the subject is beyond the scope of this text. However, consideration has been given to providing tolerance to a reasonable level of grounding inductance. The design was therefore progressed with the assumption that the grounding inductance due to assembly/packaging could be as high as 50pH, which is realistic for processes without low inductance through vias. A differential architecture benefits from a virtual earth, and this was selected to provide tolerance to the grounding inductance. It also provides rejection of common mode signals, which gives other advantages including improved second harmonic performance and higher dynamic range.

V-band amplifier stability: Although the use of a differential topology means that the grounding inductance no longer has any effect on the wanted signal, it is still very significant in common mode and can cause instability. During the design of the amplifier, measures were taken to ensure stability in differential mode, common mode and mixed mode for all frequencies up to the f_{max} of the transistors, for a grounding inductance of up to 50pH.

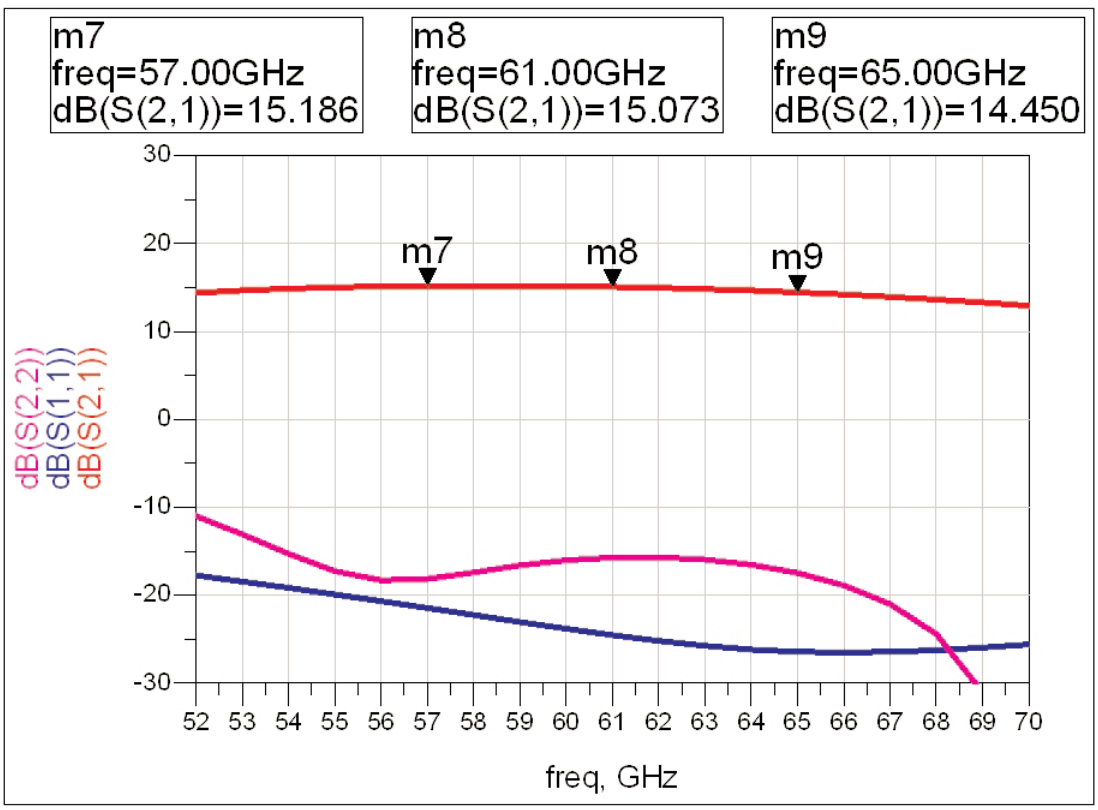

Figure 5: Small-signal performance of V-band amplifier.

A cascode architecture was adopted for the amplifying transistors. This has several benefits for millimetre-wave amplifiers implemented on SiGe, including increased voltage handling, reduced Miller capacitance, and higher isolation between input and output, making impedance matching easier and improving stability.

To achieve adequate gain a two-stage design was progressed, each stage comprising a cascode transistor arrangement. All devices were biased at 3mA/μm^2, with the devices in the second stage having twice the emitter area of those in the first. This approach ensures an adequate drive

ratio between stages, which is required for linearity.

V-band amplifier schematic: A simplified schematic showing the main elements of the first stage of the V-band amplifier is shown in Figure 4. All components are from the SG25H3 process design kit (PDK). The design makes good use of microstrip transmission lines which use a lower metal layer (metal 1) as the ground plane and an upper metal layer (top metal 2) as the conductor. Substrate losses are minimised by connecting the metal 1 ground plane to the substrate with an adequate number of p-taps in the layout. In this design the microstrip lines are essentially being used as low-value inductors. Note the use of a length of microstrip line in the tail of the differential pair — this helps to increase common mode rejection. The tail current source, traditionally used to bias differential amplifiers, was avoided, as this can lead to common mode stability problems.

Series resistors are used in the bias paths. These only affect common mode signals, and in fact contribute to providing common mode rejection and ensuring stability. The bases of the common base stage of the differential cascode are joined to form a virtual earth. Stage 2 uses a very similar topology to stage 1, with the addition of matching circuitry to transform the output impedance to 50Ω. The overall two-stage amplifier runs off a 3.3V supply and draws a total quiescent current of 24mA.

V-band amplifier performance: Typical V-band amplifier simulated performance is shown in Figures 5 and 6. The small signal gain is 14.8dB ±0.4dB across the band 57–65GHz. The output return loss is better than 15dB across the band, and the input return loss is better than 20dB across the band. The output power at 1dB gain compression is 9.5dBm ±1dB across the band.

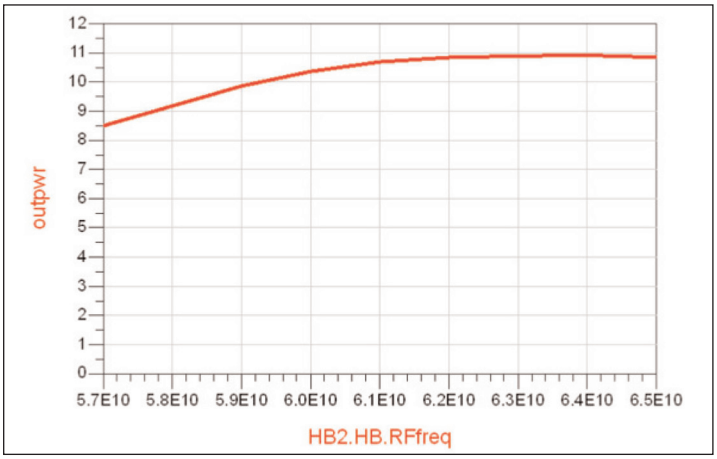

Figure 6: Output P1dB of V-band amplifier across band.

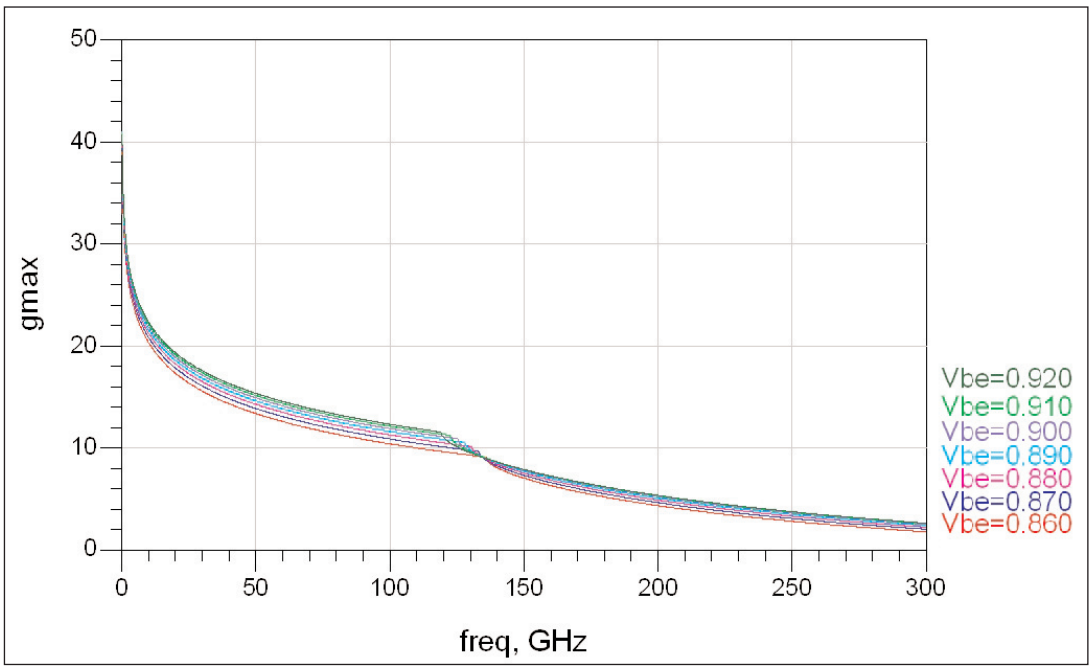

Figure 7: G_{max} versus frequency for different bias points, SG13G2 transistor.

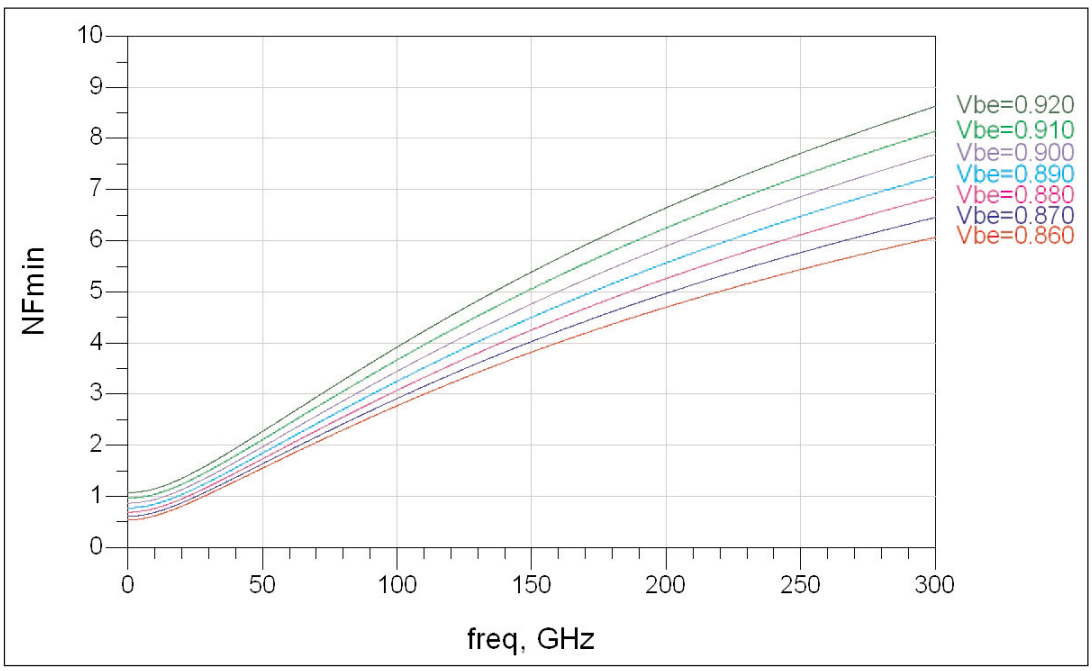

Figure 8: NF_{min} versus frequency for different bias points, SG13G2 transistor.

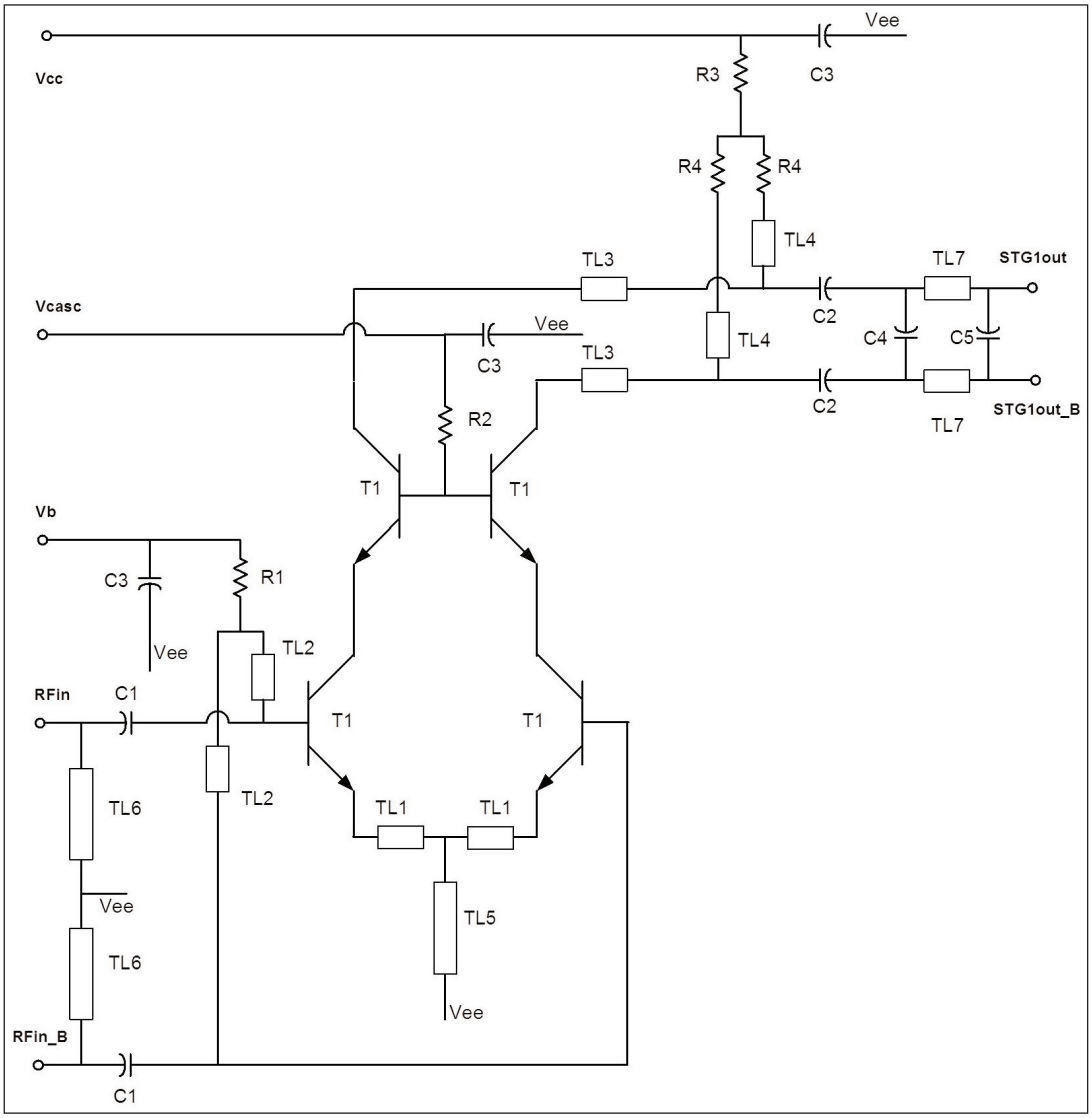

Figure 9: Simplified schematic elements of E-band amplifier first stage.

E-band IC design

Process selection: Although SG25H3 demonstrated good performance at V-band, IHP's higher f_T processes were considered more appropriate for an amplifier working at E-band (71–86GHz). After due consideration the selected process was SG13G2 which is a high performance 0.13µm technology. This offers an npn HBT with very high frequency performance (f_T/f_{max} = 300/500GHz) with a slightly lower breakdown voltage (BV_{CEO} = 1.7V).

Bias point: For peak f_T the current density for this device is around 30mA/µm^2, however, simulations of G_{max} and NF_{min} as a function of bias were carried out to gauge the bias point that would provide the best trade-off of gain for noise figure at E-band. Plots of G_{max} and NF_{min}, as a function of V_{be}, for a device in common emitter configuration with V_{ce} = 1.2V are shown in Figures 7 and 8 respectively. The emitter area is 0.07µm x 7.2µm.

A current density of 14mA/µm^2 was selected (corresponding to a typical V_{be} of 0.88V) as providing a good compromise between G_{max} and NF_{min}. The choice of V_{ce} bias of 1.2V was made considering linearity, voltage swing and device breakdown voltage. Under these quiescent conditions, the HBT dissipates 16.8mW/µm^2 which is a higher power density than that of the transistors of the V-band amplifier (5.1mW/µm^2) and requires the HBT to be implemented with a higher number of parallel devices in layout.

The 0.07µm x 7.2µm emitter area device is potentially unstable at E-band so gain must be sacrificed to ensure stability. As G_{max} for this device at the chosen bias point is high enough at the top of the band (12dB at 86GHz), this reduction in gain can be afforded.

E-band amplifier architecture: As for the V-band amplifier, the E-band amplifier was assumed to have to tolerate 50pH grounding inductance. This should provide sufficient tolerance for assembly and packaging in a real application. A similar two stage cascode architecture was adopted using a differential topology. All devices were biased at 14mA/µm^2, with the devices in the second stage having twice the emitter area as those in the first. This is to ensure an adequate drive ratio between the stages which is required for linearity.

E-band amplifier schematic: A simplified schematic showing the main elements of the E-band amplifier's first stage is depicted in Figure 9. All components are from the SG13G2 PDK. The use of the same architecture as the V-band design means that the design incorporates many similar features, including the use of microstrip transmission lines and series resistors in the bias paths. In the E-band design, however, extra loss was required differentially in the output match by means of resistors R4. As well as stabilising the stage, this loss allows for a good wideband impedance match. Although not strictly necessary, it was convenient to match the output of stage 1 to 50Ω. Stage 2 uses a very similar topology to stage 1. The E-band amplifier runs off a 2.5V supply and draws a total quiescent current of 42mA. It is stable in differential mode, common mode and mixed mode for all frequencies up to f_{max}, for up to 50pH of grounding inductance.

E-band amplifier performance: Typical E-band amplifier simulated performance is shown in Figures 10 and 11. The small-signal gain is 16.8dB ±0.9dB across the band 71–86GHz, and it exhibits a slight positive gain slope which is often a desirable feature. The output return loss is better than 16dB across the band and the input return loss is better than 17dB across the band. The output power at 1dB gain compression is 7.5dBm ±1dB across the band. Noise figure is between 4dB and 4.25dB across the band.

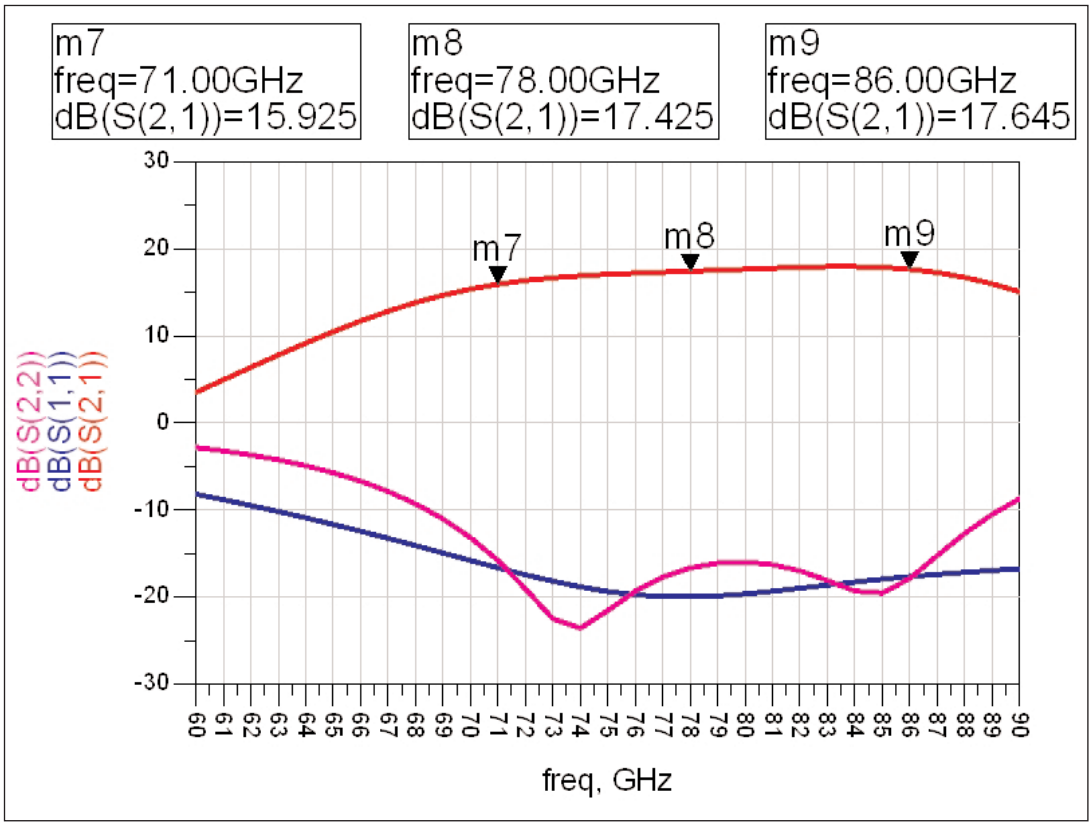

Figure 10: Small-signal performance of E-band amplifier.

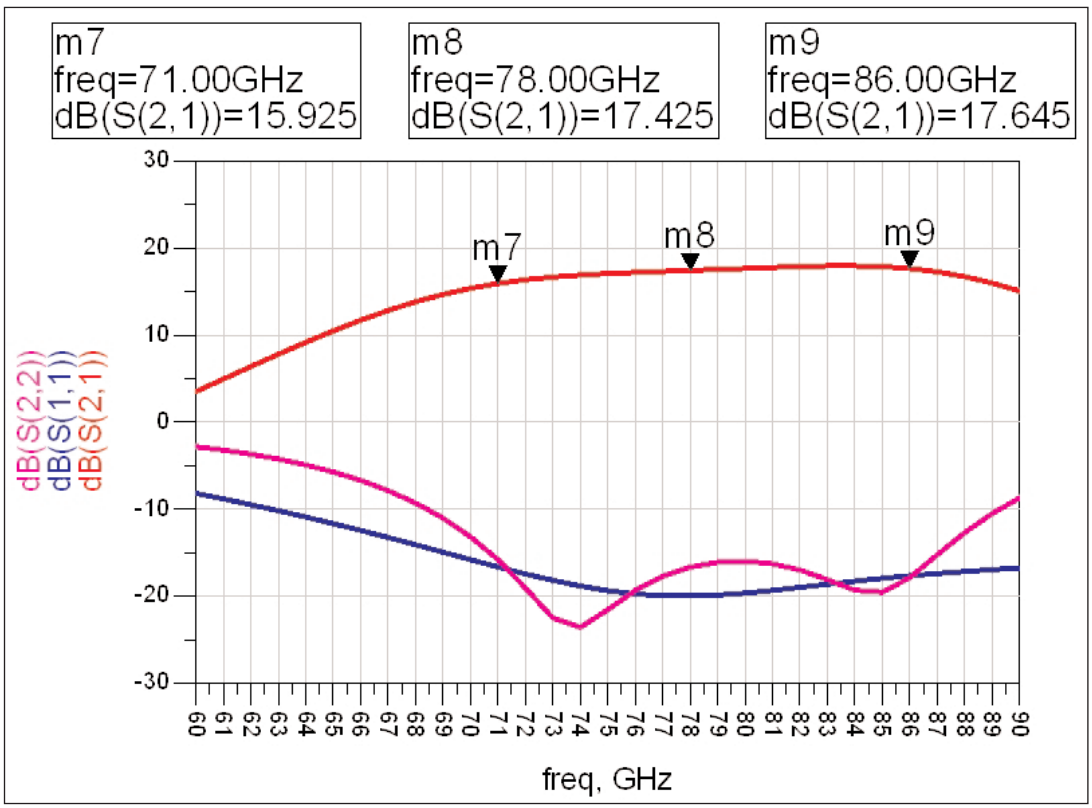

Figure 11: Output P1dB of E-band amplifier.

Conclusion

The use of SiGe technology to realize millimeter-wave ICs has been reviewed, using the examples of V-band and E-band amplifiers designed on IHP's SiGe processes to explore the implementation issues and to assess the achievable performance. Issues such as substrate loss, grounding inductance, breakdown voltage and thermal performance become more problematic at high millimeter-wave frequencies. These issues were addressed during design by appropriate choice of process, bias point and circuit architecture.

It has been noted that the potential problems that may be caused by practical levels of grounding inductance resulting from assembly and/or packaging are often inadequately covered in existing literature. The designs presented are tolerant to grounding inductances of up to 50pH, which is considered as a realistic level for a practical implementation and mandates the choice of a differential architecture. It is also vitally important to ensure amplifier stability in differential mode, common mode and mixed mode. After careful consideration of the main implementation issues, this article has demonstrated that strong performance at millimeter-wave frequencies can be achieved using IHP's SiGe processes. ■

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