

Tantalum-based ohmic contacts for nitride semiconductor transistors

Ohmic contacts developed with resistance as low as $0.06\Omega\text{-mm}$.

Sweden's Chalmers University of Technology and United Monolithic Semiconductors (UMS, a joint venture between Thales and EADS with production facilities in Orsay, France and Ulm, Germany) have been developing an alternative ohmic metal contact scheme based on tantalum (Ta) for use with aluminum gallium nitride (AlGaN) for high-electron-mobility transistors (HEMTs) [A Malmros et al, *Semicond. Sci. Technol.*, vol26, p075006, 2011]. Overall, the minimum contact resistances (R_c) found for ohmic contacts with low- and high-potential-barrier epitaxial materials were $0.06\Omega\text{-mm}$ and $0.28\Omega\text{-mm}$, respectively.

GaN HEMTs have potential applications for devices operating at high temperature, frequency and power density. Low-resistance contacts are needed for such devices to reduce losses and self-heating.

Conventional ohmic contacts in GaN HEMTs use titanium (Ti) and aluminum (Al), along with a cap to avoid oxidation of the Al layer. The cap often consists of nickel (Ni) or Ti with gold (Au). These structures require annealing at about 800°C , which can damage the performance of the semiconductor heterostructure on which the HEMT action depends. These temperatures can also melt Al, creating unwanted surface roughness of the contact.

Alternative ohmic metals for use with nitride semiconductors are being sought using molybdenum or Ta, for example, which can be annealed at lower temperatures.

The Chalmers/UMS researchers used transmission line method (TLM) structures, which are commonly used to determine the contact resistance of metal-semiconductor junctions. The TLM structures were placed on two particular epitaxial materials grown using metal-organic chemical vapor deposition (MOCVD) on silicon carbide substrates (Table 1). Such epitaxial structures are used for HEMT development.

The wafers were diced into pieces measuring $16\text{mm} \times 16\text{mm}$ before the contact metal deposition. The surfaces were prepared by degreasing, cleaning and etching into mesas. The contacts were created using photolithographic patterning and metal evaporation.

Table 1. Epitaxial heterostructures used in the experiments.

	Epi I	Epi II
Cap	GaN, 3 nm	–
Barrier	$\text{Al}_{0.14}\text{Ga}_{0.86}\text{N}$, 22 nm	$\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$, 25nm
Buffer	GaN	GaN

The metalized samples were diced further before different anneal treatments were performed.

A variety of sample structures were produced (Table 2) in two main groups with Ta/Al/Ni/Au (samples 1–4) and Ta/Al/Ta (6–17) metallization schemes. The second group (samples 6–17) was produced with the aim of creating a simpler structure and facilitating better understanding of the contact formation. The final Ta layer in the second group is used to prevent oxidation of the Al. A traditional Ti/Al/Ni/Au (sample 5) scheme was also produced for comparison purposes.

The annealing of samples was performed in an AG Heatpulse 610 rapid thermal processor (RTP) in nitrogen. Optimization of the anneal temperature was first carried out with a constant duration of 60s.

The minimum contact resistance of $0.41\Omega\text{-mm}$ for the first group of samples (1–4) occurred with sample 3 at an annealing temperature of 550°C . These results are very sensitive to the Al layer thickness, which makes process control, and hence manufacturing, difficult. The comparison stack (sample 5) became ohmic at 625°C with a minimum contact resistance of $1.63\Omega\text{-mm}$.

Ohmic contacts in GaN HEMTs use Ti and Al, along with a cap to avoid oxidation of the Al layer. The cap often consists of Ni or Ti with Au. These structures require annealing at about 800°C , which can damage the performance of the semiconductor heterostructure on which the HEMT action depends

Table 2. List of fabricated samples and the minimum R_c achieved.

Sample	Layer thickness (Å)						Thickness ratio t_{Al}/t_{Ta}	Epi	Min. R_c (Ω -mm)
	Ti	Ta	Al	Ta	Ni	Au			
1	-	100	700	-	400	400	7	I	1.36
2	-	100	1200	-	400	400	12	I	1.75
3	-	100	1400	-	400	400	14	I	0.41
4	-	100	2800	100	-	500	28	I	2.23
5	200	-	1100	-	400	400	-	I	1.63
6	-	100	700	200	-	-	7	I	0.63
7	-	100	1400	200	-	-	14	I	0.26
8	-	100	2100	200	-	-	21	I	0.65
9	-	100	2800	200	-	-	28	I	0.06
10	-	100	700	200	-	-	7	II	0.47
11	-	100	1400	200	-	-	14	II	0.54
12	-	100	2100	200	-	-	21	II	0.42
13	-	100	2800	200	-	-	28	II	0.28
14	-	50	2800	200	-	-	56	I	0.25
15	-	200	2800	200	-	-	14	I	0.49
16	-	50	2800	200	-	-	56	II	0.42
17	-	200	2800	200	-	-	14	II	1.45

These results were all obtained with the 'epi I' structure with a 14%-Al AlGaN barrier and 3nm GaN cap layer.

The same epi I structure with Ta/Al/Ta metallization (samples 6–9) showed much less sensitivity to the Al layer thickness. The best value of contact resistance of 0.06 Ω -mm for sample 9 was achieved with an annealing temperature of 550°C.

Samples 10–13 on the epi II structure, with 25%-Al AlGaN barrier and no GaN cap, exhibited the lowest contact resistance of 0.42 Ω -mm at 600°C. In the last sequence of samples (14–17), where the bottom Ta layer thickness was varied, the minimum contact resistance was also achieved at 600°C.

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From this point, the researchers focused on the stack without Ni-Au, seeing the use of these metals as being an 'unnecessary, complicating factor'.

The anneal duration was then varied at a temperature of 550°C (Figure 1). The results suggest that the epi II structure requires longer duration to anneal the Ta/Al/Ta stack.

On the basis of comparing the minimum contact resistances with the thickness ratios for the Ta and Al ratios, the researchers comment: "Both heterostructures exhibited the minimum R_c at a t_{Al}/t_{Ta} of 28, which may indicate that this value is close to optimum". However, they also believe that more work is needed to confirm this.

The researchers also studied the sheet resistance of the epitaxial material, which needs to be maintained for transistor performance. The value remained stable at 980 Ω /square for epi I up to 575°C. Epi II maintained its sheet resistance to higher anneal temperatures — sample 11 had an increase in sheet resistance from its normal value of 420 Ω /square to 500 Ω /square after annealing at 650°C for 60s.

SEM and optical analysis showed smooth surfaces of the metal layers up to 600°C. At higher temperatures the surface morphology became rougher. Smoother morphology would facilitate lateral scaling/size reduction of devices.

Further work involved transmission electron microscopy (TEM) and energy-dispersive x-ray (EDX) spectroscopy. These studies suggested that interdiffusion of metals with Ta/Al/Ni/Au metallization caused the poor performance of this sequence. On the basis of their analysis, the researchers believe that the contact

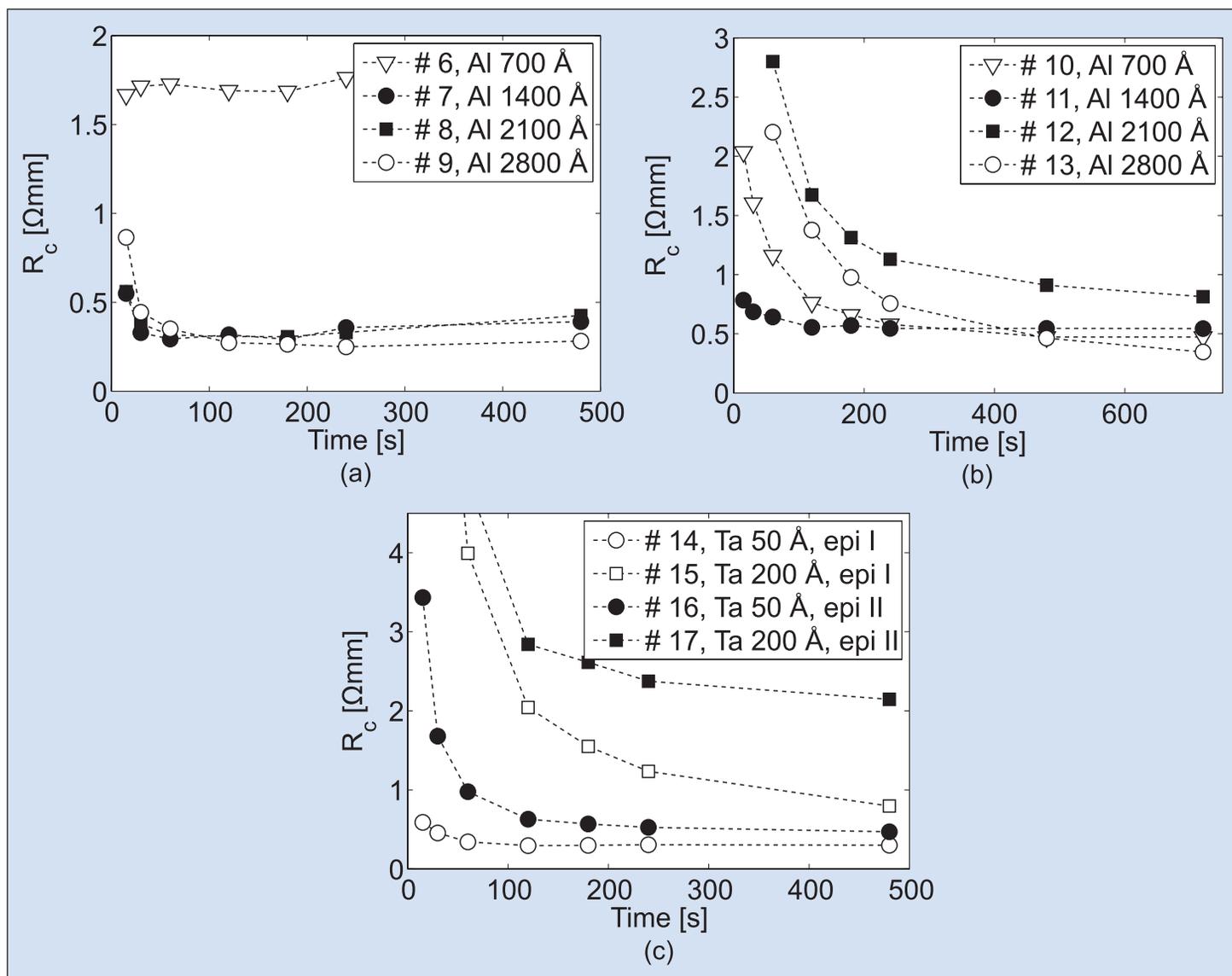


Figure 1. R_c versus time of annealing at 550°C for samples 6–17: (a) Ta/Al/Ta metallization on epi I, (b) Ta/Al/Ta metallization on epi II and (c) Ta/Al/Ta metallization on epi I and II with different Ta layer thicknesses.

mechanism is due to the formation of a metal-nitrogen compound at the metal–semiconductor interface, causing donor-like nitrogen vacancies in the semiconductor.

Thermal stability of the contacts was studied by storing samples 7 and 9 in air at 300°C. They maintained their initial contact resistance values for more than 400

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hours. However, there was an increase in the epitaxial structure's sheet resistance of 6–8% over the test period.

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