CEA-Leti proof of concept demonstrates higher electron mobility in GeSn than in silicon or germanium

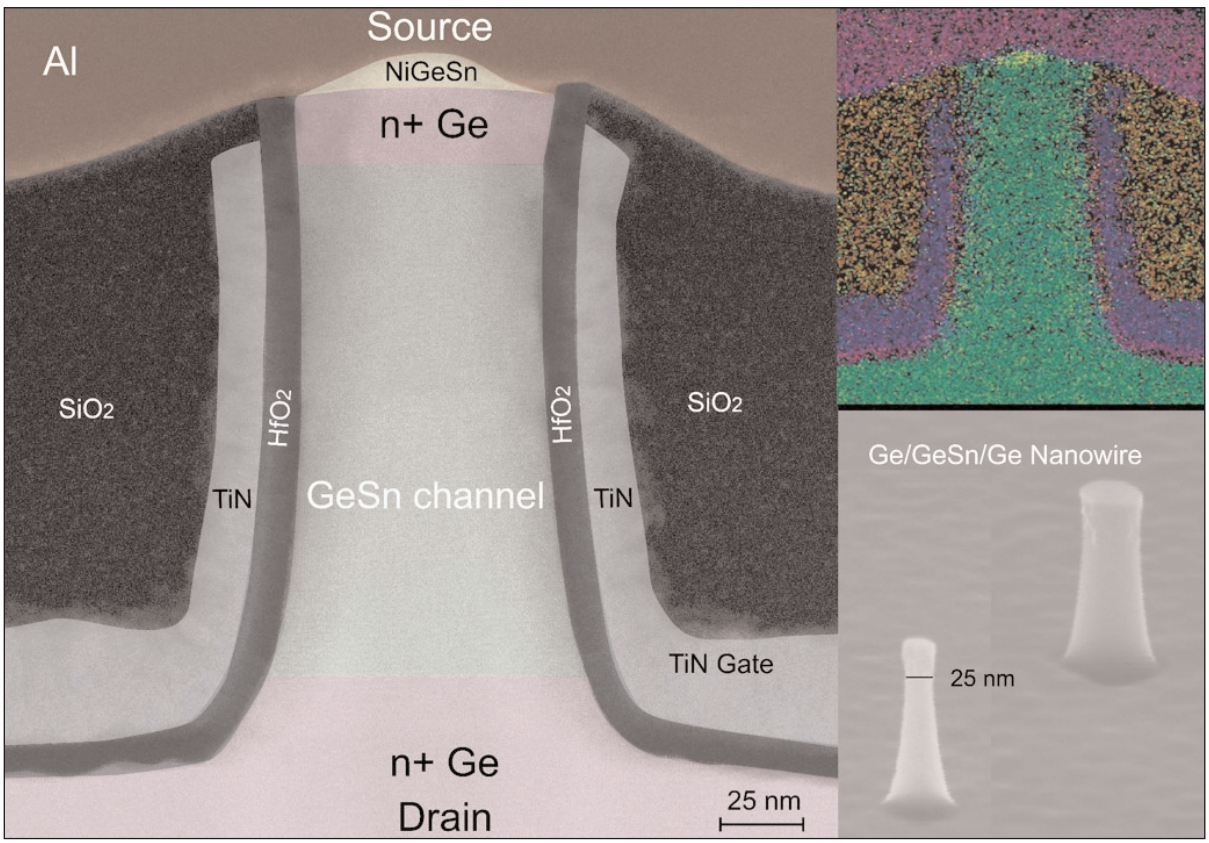
Vertical GeSn transistors may enable low-power, high-performance chips and quantum computers.

Micro/nanotechnology R&D center CEA-Leti of Grenoble, France has demonstrated that electrons and other charge carriers can move faster in germanium tin than in silicon or germanium, enabling lower operation voltages and smaller footprints in vertical devices than in planar devices. This proof-of-concept means that vertical transistors made of germanium tin are promising candidates for future low-power, high-performance chips and possibly quantum computers.

Germanium–tin transistors have an electron mobility that is 2.5 times higher than a comparable transistor made of pure germanium. GeSn is otherwise compatible with existing CMOS chip fabrication processes. Because both germanium and tin come from the same group of the periodic table as silicon, these transistors could be integrated directly into conventional silicon chips with existing production lines.

The paper 'Vertical GeSn Nanowire MOSFETs for CMOS Beyond Silicon' (Mingshan Liu et al, Nature Communications Engineering volume 2, article number 7 (2023)) notes that "GeSn alloys offer a tunable energy bandgap by varying the Sn content and adjustable band off-sets in epitaxial heterostructures with Ge and SiGe. In fact, a recent report has shown that the use of $Ge_{0.92}Sn_{0.08}$ as source on top of Ge nanowires (NWs) enhances the p-MOSFET performances."

"In addition to their unprecedented electro-optical properties, a major advantage of GeSn binaries is also that they can be grown in the same epitaxy reactors as Si and SiGe alloys, enabling an all-group IV optoelec-



Cross sectional transmission electron microscopy image of a vertical GeSn/Ge gate-all-around (GAA) nanowire FET, with (inset top-right) energy-dispersive x-ray (EDX) elemental mapping (showing Sn in green and Ti in blue) and (inset bottom-right) overlapped SEM images of GeSn/Ge nanowires used for p-VFETs.

tronic semiconductor platform that can be monolithically integrated on silicon," the paper adds.

That project research included contributions from several organizations in addition to CEA-Leti, which delivered the epitaxial stacks. Epitaxy is carried out on a very ordered template, a silicon substrate, with a very precise crystal structure. By changing the material, CEA-Leti duplicated its diamond crystalline structure in the layers it grew on top.

Epitaxy is performed at low temperature in a chemical vapor deposition (CVD) reactor, notes Jean-Michel Hartmann, a CEA Fellow, leader of the working group on IV epitaxy at CEA-Leti, and scientific director of the SSURF department.

Epitaxial layer deposition of this kind of stack is a complex step in a process flow requiring patterned cylinders and conformal gate stack deposition. CEA-Leti claims to be one of the few RTOs (research and technology organizations) globally that is able to deposit such complex in-situ-doped Ge/GeSn stacks.

"The collaboration demonstrated the potential of low-bandgap GeSn for advanced transistors with interesting electrical properties, such as high carrier mobilities in the channel, low operating voltages and a smaller footprint," says Hartmann, a co-author of the paper. "Industrialization is still far away. We are advancing on the state of the art and showing the potential of germanium tin as a channel material."

The work also included scientists from ForschungsZentrum Jülich in Germany; the University of Leeds in the UK; IHP- Innovations for High Performance Microelectronics in Frankfurt (Oder), and RWTH Aachen University in Germany.

Hartmann received the Electronics and Photonics Division Award at the recent Electrochemical Society conference in Boston, MA, USA. As the honoree, on 30 May Hartmann presented a paper 'Epitaxy of Group-IV Semiconductors for Nanoelectronics and Optoelectronics' covering how epitaxy can be put to good use to boost properties of devices. Hartmann's research focuses on the reduced-pressure chemical vapor deposition (RP-CVD) of group-IV semiconductors for nanoelectronics and optoelectronics. ■

Jean-Michel Hartmann, leader of the working group on IV epitaxy at CEA-Leti, receiving the Electronics and Photonics Division Award at the Electrochemical Society conference.

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