Dynamic performance of vertical GaN JFETs

First study shows no shift in R_{ON} or V_{TH}, according to researchers.

Virginia Polytechnic Institute and State University and NexGen Power Systems Inc in the USA have claimed the first experimental characterization of dynamic on-resistance (R_{ON}) and threshold voltage (V_{TH}) stability in vertical gallium nitride (GaN) power transistors [Xin Yang et al, IEEE Transactions On Electron Devices, vol.71, issue 1 (January 2024), p720]. The researchers studied NexGen junction field-effect transistor (JFET) devices rated at up to 1200V (1.2kV).

Dynamic R_{ON} describes the increased resistance of switched transistors relative to the value in a steady DC state. The team comments: "This issue can induce a higher conduction loss of the device and a degraded device lifetime in applications."

The researchers compared the performance of NexGen's 650V/200mΩ- and 1200V/70mΩ-rated GaN JFETs (Figure 1) against that of commercial 650V and 1200V silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs, IMZA65R083M1H, C3M0075120D), and 650V GaN high-electron-mobility transistor with Schottky-type p-GaN gate (SP-HEMT, GS-065-011-1-L).

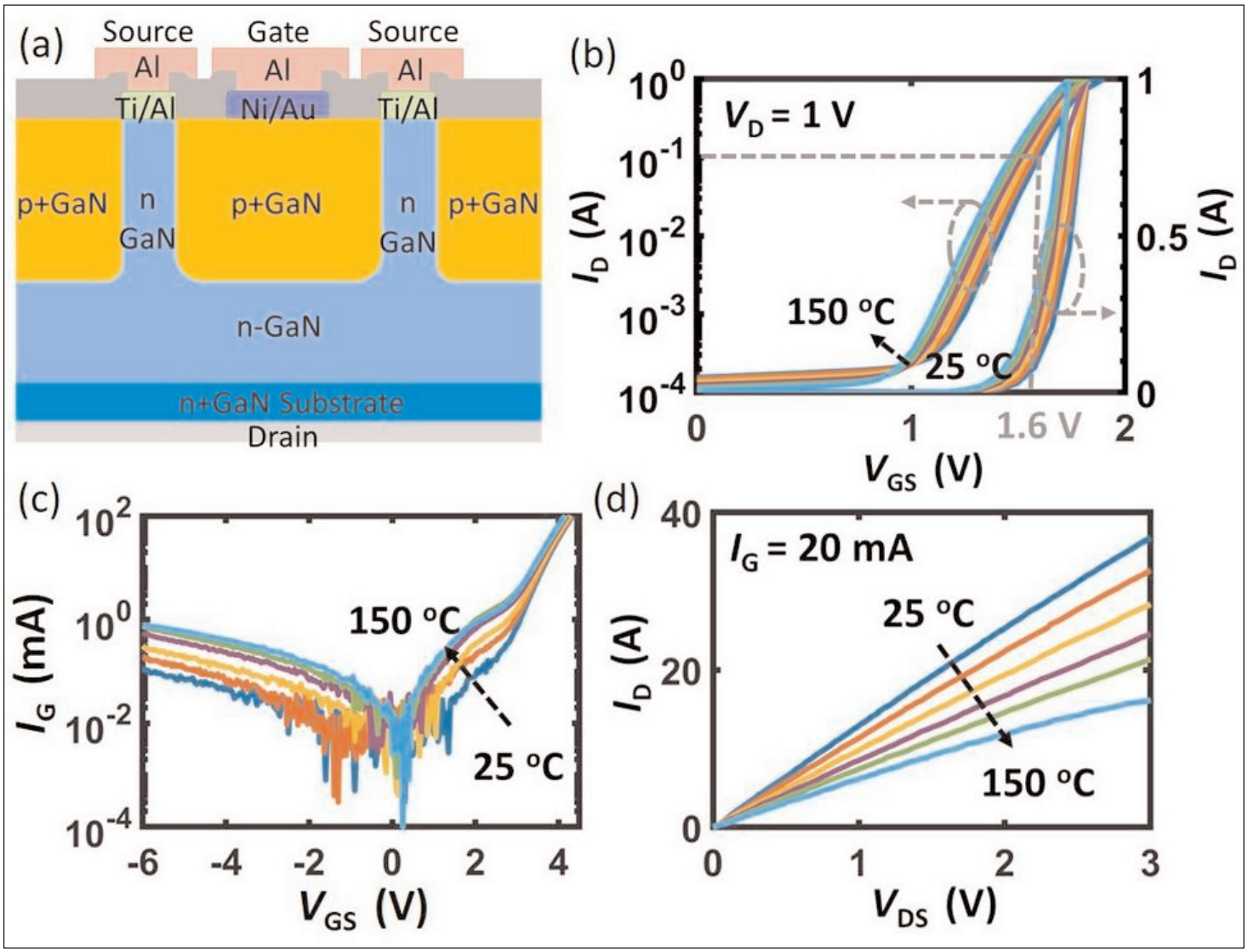

Figure 1. (a) Schematic of vertical GaN JFET. Characteristics at 25-150°C with 25°C incremental step of 1.2kV device: (b) transfer, drain current (I_D) versus gate potential (V_{GS}) on log and linear scales; (c) I_G versus V_{GS}; and (d) output.

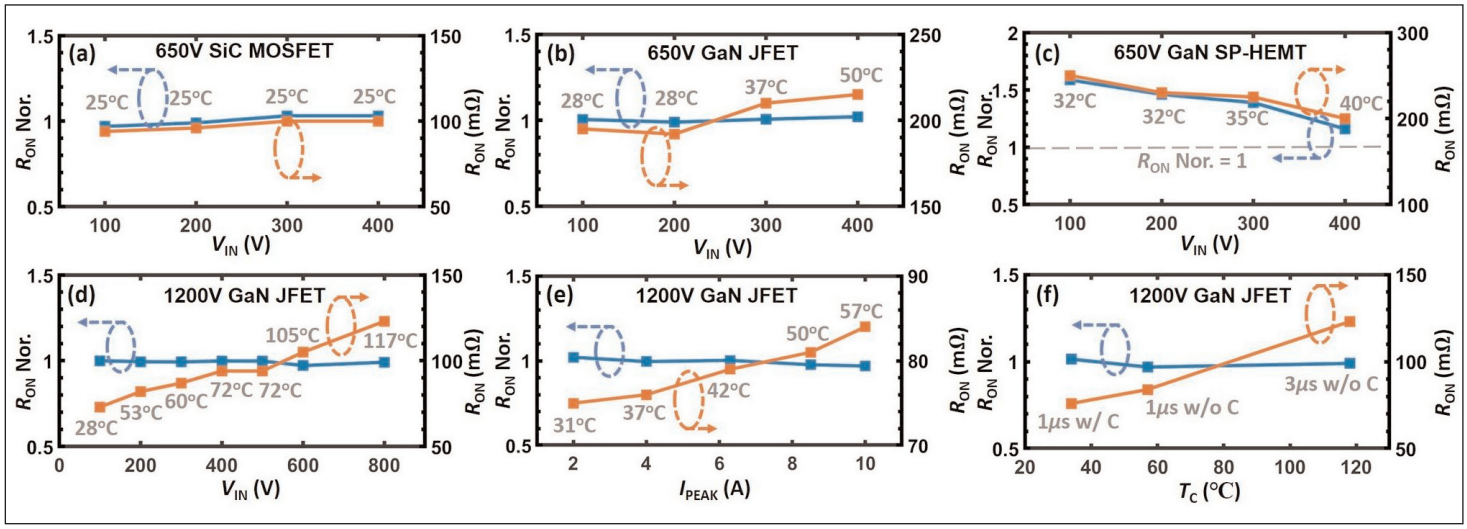

Figure 2. Extracted dynamic R_{ON} and normalized dynamic R_{ON} versus V_{IN} with 3µs pulse width for 650V-rated (a) SiC MOSFET, (b) GaN JFET, (c) GaN SP-HEMT, and (d) 1200V GaN JFET. (e) and (f) Dynamic R_{ON} performance of 1200V GaN JFET at 800V V_{IN} (10A steady state) versus 1µs pulse peak drain current and T_C with/without cooling, respectively.

NexGen's devices were fabricated on 100mm bulk n^+-GaN substrates. The fin channels were around 1µm high and sub-micron in width. The gate consisted of implanted p-GaN regions between the fins. The drift region between the fin channels and the drain was around 8µm and 10µm for the 650V and 1200V devices, respectively. The corresponding avalanche breakdown voltages were estimated to be 800V and 1500V.

The threshold voltage (V_{TH}) of the 1.2kV JFET was 1.6V at 25°C, decreasing to 1.45V at 150°C. The R_{ON} at 20mA IG was around 70mΩ at 25°C, increasing to 150mΩ at 150°C.

The researchers used continuous, hard-switching double pulse tests (DPTs) with an active measurement circuit to assess the dynamic R_{ON} performance (Figure 2). The devices were assembled in dual flat no-lead (DFN) packages, and case temperature (TC) was determined using thermal imaging. Fan cooling was applied to the SiC MOSFET and GaN SP-HEMT comparison devices, but not to the GaN JFETs. The R_{ON} values were normalized according to the static R_{ON} at the measured T_C.

The researchers comment: "The results show 650V and 1200V GaN JFETs are both dynamic R_{ON} free."

The researchers also performed static stress testing to determine how stable the R_{ON} and V_{TH} values were, as relevant to application scenarios where the power device is mostly off. The maximum V_{TH} and R_{ON} shifts for the 1200V JFET were 0.05% and 1.38%, respectively. By contrast, a 650V GaN SP-HEMT has corresponding shifts of order 20% and 10%.

The researchers also compared simulations of JFET and HEMT structures to analyze the difference in dynamic R_{ON} and static stability performance. The team suggests that a key difference arises in the position of the peak electric field, which usually arises near the edge termination. In the HEMT structure, the peak field is only 20–30nm from the device surface, while in the JFET peak E is buried about a 1µm away from the surface. Combined with the lower defect density in epitaxial layers grown on bulk GaN, surface and buffer traps are largely suppressed, reducing delays in state changes, which almost eliminates the dynamic R_{ON} in the GaN JFET, it is thought.

The researchers add: "Finally, the native p-n junction gate in JFET has no band discontinuities, enabling the more efficient carrier supply or extraction as compared to the p-GaN/AlGaN/GaN hetero-gate in the HEMTs (particularly with the Schottky contact to p- GaN in SP-HEMT)." ■

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